Discussion 6

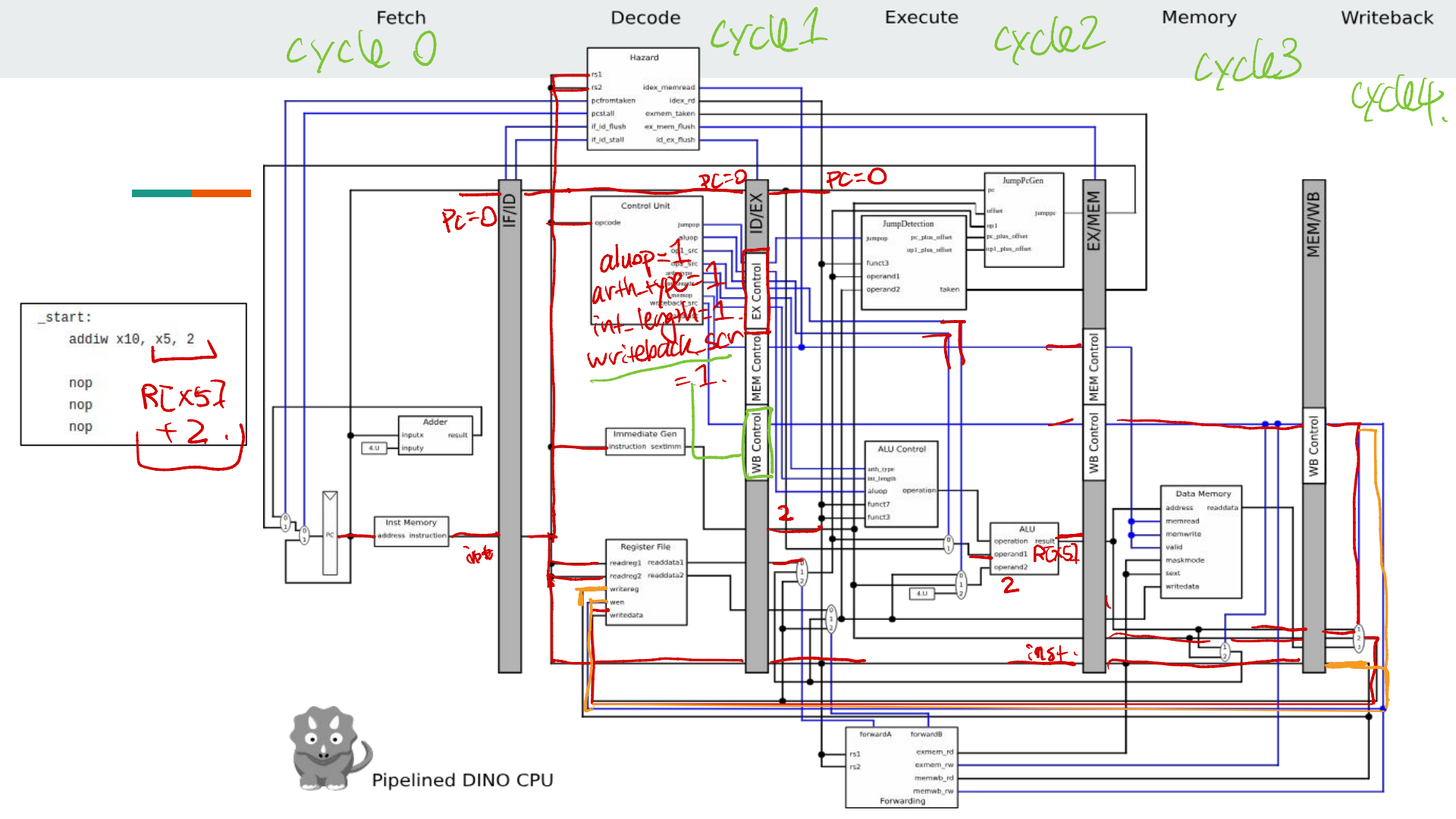
Feb 13

Outline

- DINOCPU assignment 3.1
  - addiw2
- DINOCPU assignment 3.2
  - swfwd1
  - lwfwd
  - beq-True

addiw2

```
_start:
    addiw x10, x5, 2
    nop
    nop
    nop
```


Fetch
Decode
Execute
Memory
Writeback
cycle 0
cycle 1
cycle2
cycle3
cycle4.
_start:
addiw x10, x5, 2
nop
nop
nop
R[x5]
+2.
Hazard
Control Unit
IF/ID
ID/EX
EX/MEM
MEM/WB
EX Control
MEM Control
WB Control
JumpPcGen
JumpDetection
Adder
Immediate Gen
Inst Memory
Register File
ALU Control
ALU
Data Memory
Forwarding
forwardA
forwardB
PC=0
aluop=1
arth_type=1
int_length=1
writeback_scr
=1.
R[5]
inst.
Pipelined DINO CPU

Cycle 0

```
Single stepper> print piperegs
if_id.pc                                0 (0x0)
if_id.instruction                       0 (0x0)
if_id.instruction (input)               2262299 (0x22851b)
if_id.pc (input)                        0 (0x0)
```

```
imem.good                       1 (0x1)
imem.ready                      1 (0x1)
imem.instruction                81606640923 (0x130022851b)
imem.valid                      1 (0x1)
imem.address                    0 (0x0)
```

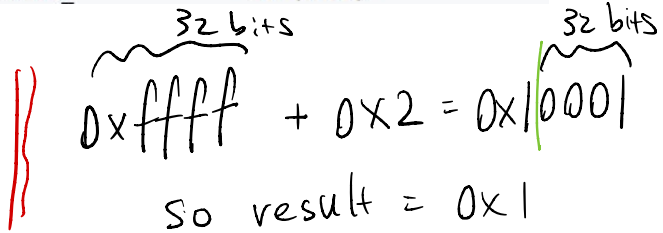
Cycle 1

```
Current cycle: 1
Single stepper> dump control
control.io.memop                0 (0x0)
control.io.op2_src              1 (0x1)
control.io.op1_src              0 (0x0)
control.io.jumpop               0 (0x0)
control.io.aluop                1 (0x1)
control.io.int_length           1 (0x1)
control.io.arth_type            1 (0x1)
control.io.writeback_src        1 (0x1)
control.io.opcode               27 (0x1b)
Single stepper> dump immGen
immGen.io.instruction           2262299 (0x22851b)
immGen.io.sextImm               2 (0x2)
Single stepper> dump registers
registers.io.readdata1          4294967295 (0xffffffff)
registers.io.readdata2          0 (0x0)
registers.io.readreg1           5 (0x5)
registers.io.writereg           0 (0x0)
registers.io.readreg2           2 (0x2)
registers.io.writedata          0 (0x0)
registers.io.wen                0 (0x0)
```

```
if_id.pc                                0 (0x0)
if_id.instruction                       2262299 (0x22851b)
if_id.instruction (input)               19 (0x13)
if_id.pc (input)                        4 (0x4)
id_ex.instruction                       0 (0x0)
id_ex.readdata2                         0 (0x0)
id_ex.pc                                0 (0x0)
id_ex.readdata1                         0 (0x0)
id_ex.sextImm                           0 (0x0)
id_ex.instruction (input)               2262299 (0x22851b)
id_ex.pc (input)                        0 (0x0)
id_ex.readdata1 (input)                 4294967295 (0xffffffff)
id_ex.sextImm (input)                   2 (0x2)
id_ex.readdata2 (input)                 0 (0x0)
id_ex_ctrl.ex_ctrl_arth_type            0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src              0 (0x0)
id_ex_ctrl.mem_ctrl_memop               0 (0x0)
id_ex_ctrl.ex_ctrl_aluop                0 (0x0)
id_ex_ctrl.ex_ctrl_jumpop               0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src        0 (0x0)
id_ex_ctrl.ex_ctrl_int_length           0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src              0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src (input)      0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src (input)1 (0x1)
id_ex_ctrl.ex_ctrl_arth_type (input)    1 (0x1)
id_ex_ctrl.ex_ctrl_aluop (input)        1 (0x1)
id_ex_ctrl.ex_ctrl_jumpop (input)       0 (0x0)
id_ex_ctrl.ex_ctrl_int_length (input)   1 (0x1)
id_ex_ctrl.ex_ctrl_op2_src (input)      1 (0x1)
id_ex_ctrl.mem_ctrl_memop (input)       0 (0x0)
```

Cycle 2

```
Single stepper> dump aluControl
aluControl.io.int_length        1 (0x1)
aluControl.io.funct3            0 (0x0)
aluControl.io.arth_type         1 (0x1)
aluControl.io.aluop             1 (0x1)
aluControl.io.funct7            0 (0x0)
aluControl.io.operation         16 (0x10)
Single stepper> dump alu
alu.io.operand1                 4294967295 (0xffffffff)
alu.io.result                   1 (0x1)
alu.io.operand2                 2 (0x2)
alu.io.operation_               16 (0x10)
```




```
id_ex.instruction               2262299 (0x22851b)
id_ex.readdata2                 0 (0x0)
id_ex.pc                        0 (0x0)
id_ex.readdata1                 4294967295 (0xffffffff)
id_ex.sextImm                   2 (0x2)
id_ex.instruction (input)       19 (0x13)
id_ex.pc (input)                4 (0x4)
id_ex.readdata1 (input)         0 (0x0)
id_ex.sextImm (input)           0 (0x0)
id_ex.readdata2 (input)         0 (0x0)
id_ex_ctrl.ex_ctrl_arth_type    1 (0x1)
id_ex_ctrl.ex_ctrl_op2_src      1 (0x1)
id_ex_ctrl.mem_ctrl_memop       0 (0x0)
id_ex_ctrl.ex_ctrl_aluop        1 (0x1)
id_ex_ctrl.ex_ctrl_jumpop       0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src 1 (0x1)
id_ex_ctrl.ex_ctrl_int_length   1 (0x1)
id_ex_ctrl.ex_ctrl_op1_src      0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src (input) 0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src (input)1 (0x1)
id_ex_ctrl.ex_ctrl_arth_type (input) 1 (0x1)
id_ex_ctrl.ex_ctrl_aluop (input) 1 (0x1)
id_ex_ctrl.ex_ctrl_jumpop (input) 0 (0x0)
id_ex_ctrl.ex_ctrl_int_length (input) 0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src (input) 1 (0x1)
id_ex_ctrl.mem_ctrl_memop (input) 0 (0x0)
ex_mem.alu_result               0 (0x0)
ex_mem.mem_writedata            0 (0x0)
ex_mem.sextImm                  0 (0x0)
ex_mem.taken                    0 (0x0)
ex_mem.jumppc                   0 (0x0)
ex_mem.instruction              0 (0x0)
ex_mem.sextImm (input)          2 (0x2)
ex_mem.instruction (input)      2262299 (0x22851b)
ex_mem.taken (input)            0 (0x0)
ex_mem.alu_result (input)       1 (0x1)
ex_mem.jumppc (input)           0 (0x0)
ex_mem.mem_writedata (input)    0 (0x0)
ex_mem_ctrl.mem_ctrl_memop      0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src 0 (0x0)
ex_mem_ctrl.mem_ctrl_memop (input) 0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src (input)1 (0x1)
```

Cycle 3

```
Current cycle: 3
Single stepper> dump dmem
dmem.valid                          0 (0x0)
dmem.readdata                       0 (0x0)
dmem.memread                        0 (0x0)
dmem.good                           1 (0x1)
dmem.maskmode                       0 (0x0)
dmem.sext                           1 (0x1)
dmem.address                        1 (0x1)
dmem.memwrite                       0 (0x0)
dmem.writedata                      0 (0x0)
```

```
ex_mem.alu_result                          1 (0x1)
ex_mem.mem_writedata                       0 (0x0)
ex_mem.sextImm                             2 (0x2)
ex_mem.taken                               0 (0x0)
ex_mem.jumppc                              0 (0x0)
ex_mem.instruction                         2262299 (0x22851b)
ex_mem.sextImm (input)                     0 (0x0)
ex_mem.instruction (input)                 19 (0x13)
ex_mem.taken (input)                       0 (0x0)
ex_mem.alu_result (input)                  0 (0x0)
ex_mem.jumppc (input)                      0 (0x0)
ex_mem.mem_writedata (input)               0 (0x0)
ex_mem_ctrl.mem_ctrl_memop                 0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src          1 (0x1)
ex_mem_ctrl.mem_ctrl_memop (input)         0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src (input)1 (0x1)
mem_wb.mem_readdata                        0 (0x0)
mem_wb.instruction                         0 (0x0)
mem_wb.alu_result                          0 (0x0)
mem_wb.sextImm                             0 (0x0)
mem_wb.alu_result (input)                  1 (0x1)
mem_wb.mem_readdata (input)                0 (0x0)
mem_wb.sextImm (input)                     2 (0x2)
mem_wb.instruction (input)                 2262299 (0x22851b)
mem_wb_ctrl.wb_ctrl_writeback_src          0 (0x0)
mem_wb_ctrl.wb_ctrl_writeback_src (input)1 (0x1)
```

Cycle 4

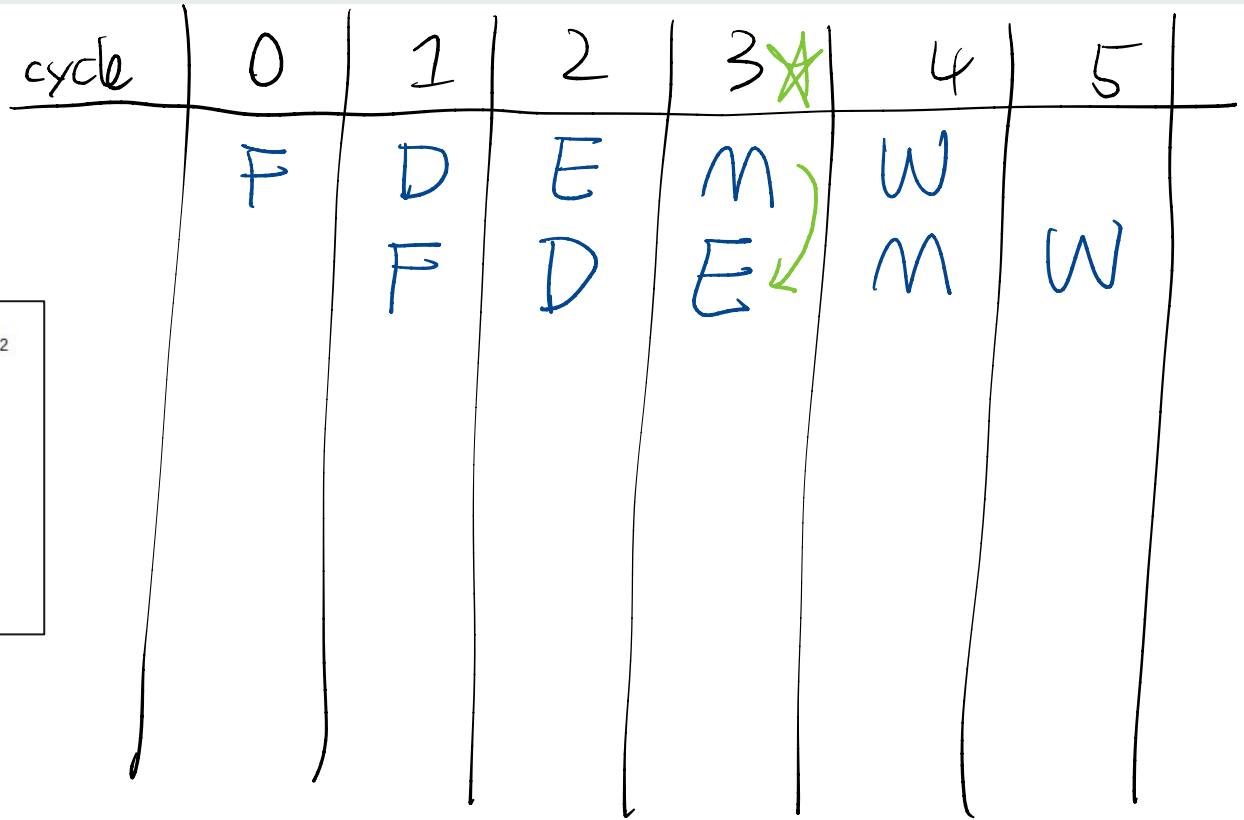
```
Current cycle: 4
Single stepper> dump registers
registers.io.readdata1          0 (0x0)
registers.io.readdata2          0 (0x0)
registers.io.readreg1           0 (0x0)
registers.io.writereg           10 (0xa)
registers.io.readreg2           0 (0x0)
registers.io.writedata          1 (0x1)
registers.io.wen                1 (0x1)
```

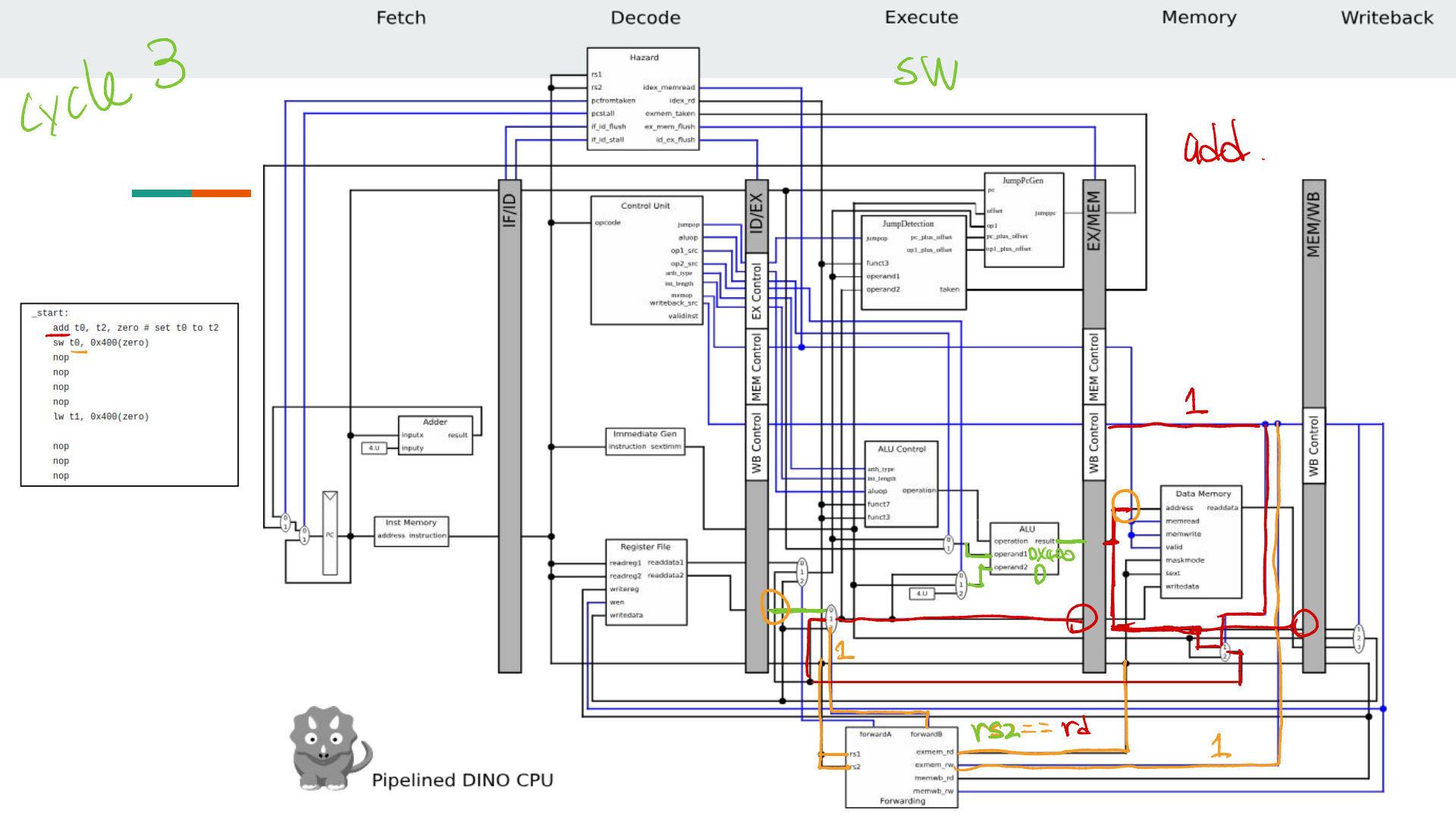
```
mem_wb.mem_readdata                          0 (0x0)
mem_wb.instruction                           2262299 (0x22851b)
mem_wb.alu_result                            1 (0x1)
mem_wb.sextImm                               2 (0x2)
mem_wb.alu_result (input)                    0 (0x0)
mem_wb.mem_readdata (input)                  0 (0x0)
mem_wb.sextImm (input)                       0 (0x0)
mem_wb.instruction (input)                   19 (0x13)
mem_wb_ctrl.wb_ctrl_writeback_src            1 (0x1)
mem_wb_ctrl.wb_ctrl_writeback_src (input)1 (0x1)
```

swfwd1

```
_start:
    add t0, t2, zero # set t0 to t2
    sw t0, 0x400(zero)
    nop
    nop
    nop
    nop
    lw t1, 0x400(zero)

    nop
    nop
    nop
```




Fetch
Decode
Execute
Memory
Writeback
cycle 3
sw
add.
_start:
add t0, t2, zero # set t0 to t2
sw t0, 0x400(zero)
nop
nop
nop
nop
lw t1, 0x400(zero)
nop
nop
nop
Hazard
rs1
rs2
pcfromtaken
pcstall
if_id_flush
if_id_stall
idex_memread
idex_rd
exmem_taken
ex_mem_flush
id_ex_flush
IF/ID
ID/EX
EX/MEM
MEM/WB
Control Unit
opcode
jumpop
aluop
op1_src
op2_src
arth_type
ins_length
memop
writeback_src
validinst
EX Control
MEM Control
WB Control
JumpPcGen
pc
offset
jumppc
op1
pc_plus_offset
op1_plus_offset
JumpDetection
jumpop
funct3
operand1
operand2
taken
Adder
inputx
inputy
result
4.U
Immediate Gen
instruction
sextImm
Inst Memory
address
instruction
pc
Register File
readreg1
readreg2
writereg
wen
writedata
readdata1
readdata2
ALU Control
operation
funct7
ALU
result
Data Memory
memread
memwrite
valid
maskmode
sext
forwardA
forwardB
exmem_rd
exmem_rw
memwb_rd
memwb_rw
Forwarding
1
rs2 == rd
Pipelined DINO CPU

Cycle 3

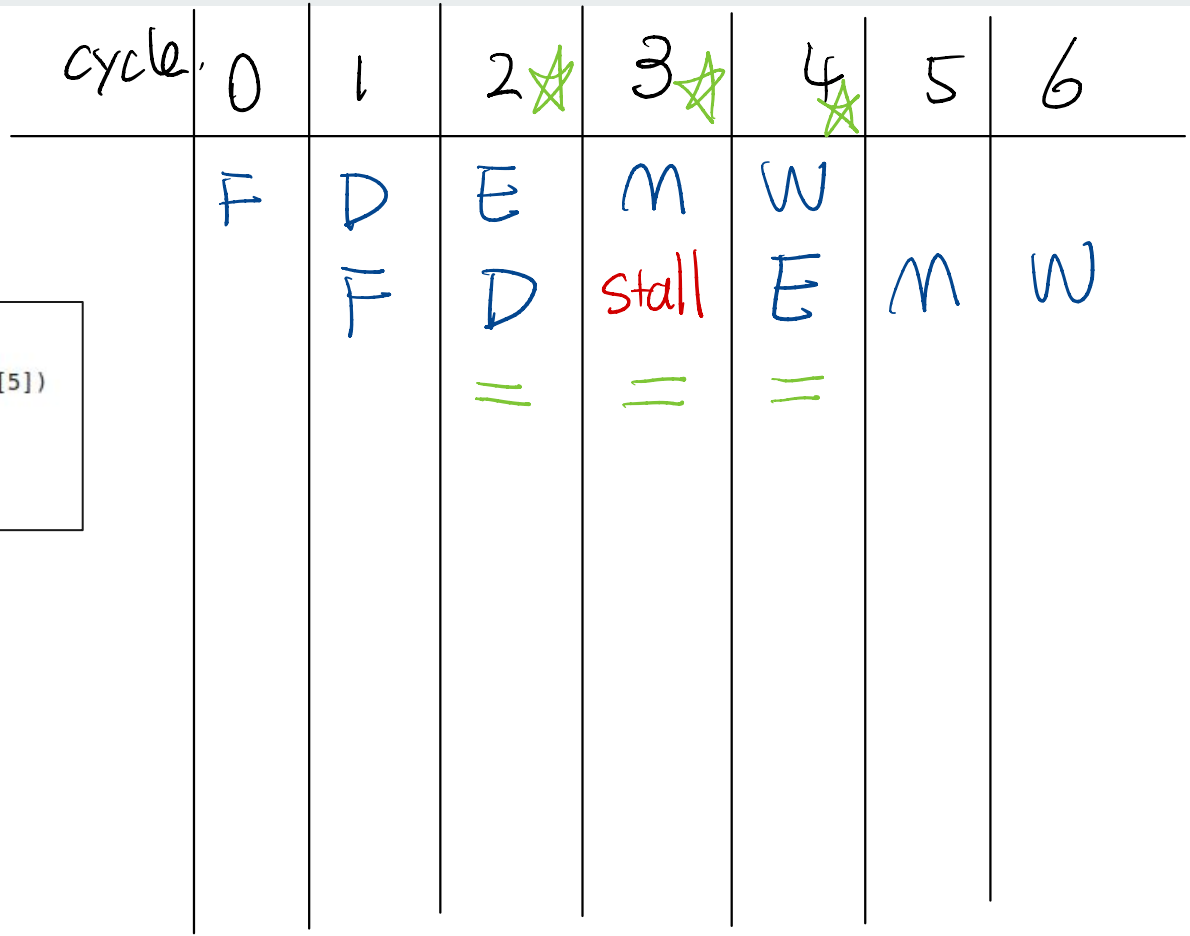
```
forwarding.io.memwbrd                0 (0x0)
forwarding.io.memwbrw                0 (0x0)
forwarding.io.forwardB               1 (0x1)
forwarding.io.forwardA               0 (0x0)
forwarding.io.exmemrd                5 (0x5)
forwarding.io.rs1                    0 (0x0)
forwarding.io.rs2                    5 (0x5)
forwarding.io.exmemrw                1 (0x1)
```

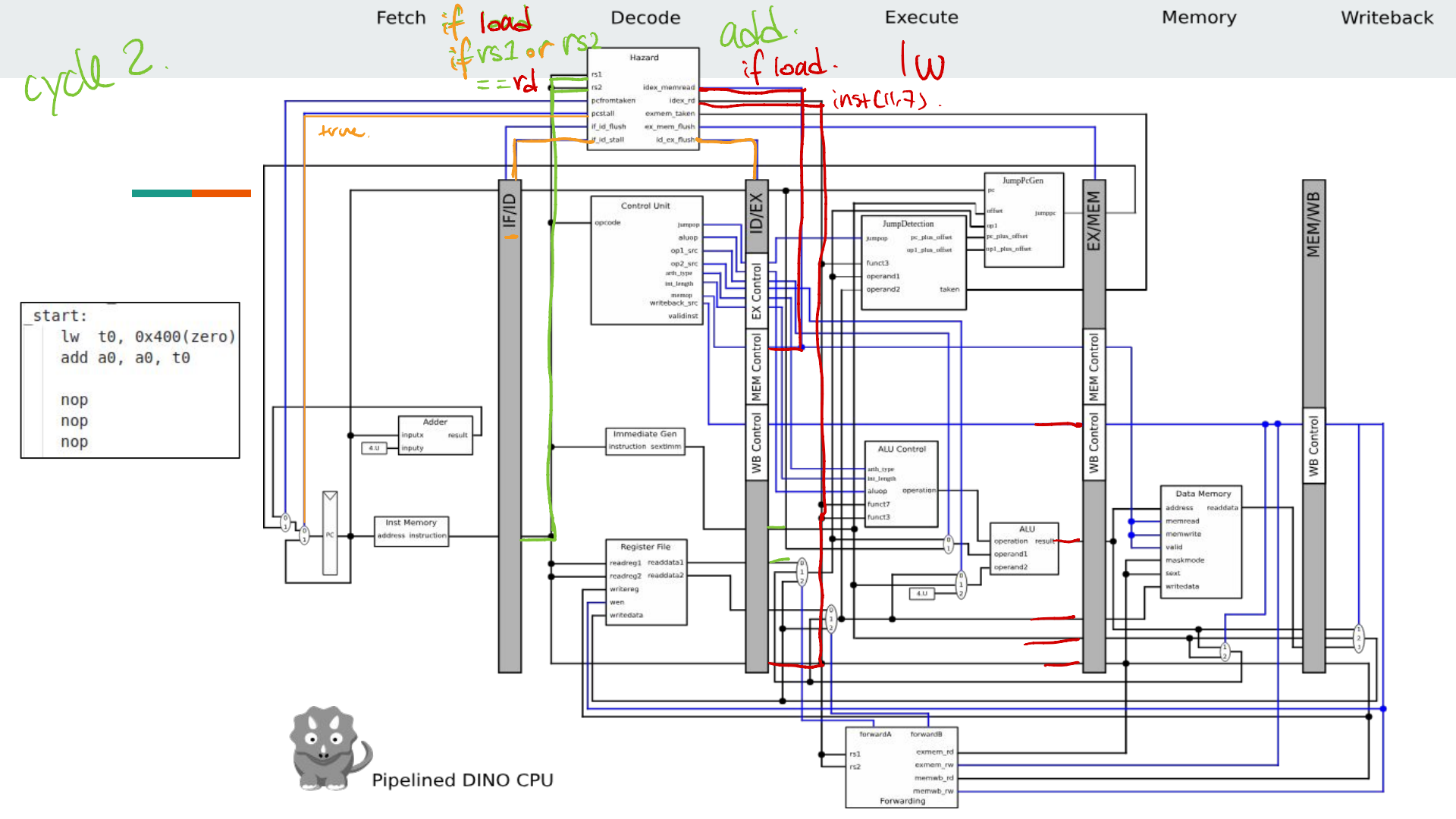
```
ex_mem.alu_result                          1234 (0x4d2)
ex_mem.mem_writedata                       0 (0x0)
ex_mem.sextImm                             0 (0x0)
ex_mem.taken                               0 (0x0)
ex_mem.jumppc                              0 (0x0)
ex_mem.instruction                         230067 (0x382b3)
ex_mem.sextImm (input)                     1024 (0x400)
ex_mem.instruction (input)                 1078992931 (0x40502023)
ex_mem.taken (input)                       0 (0x0)
ex_mem.alu_result (input)                  1024 (0x400)
ex_mem.jumppc (input)                      0 (0x0)
ex_mem.mem_writedata (input)               1234 (0x4d2)
ex_mem_ctrl.mem_ctrl_memop                 0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src          1 (0x1)
ex_mem_ctrl.mem_ctrl_memop (input)         2 (0x2)
ex_mem_ctrl.wb_ctrl_writeback_src (input)0 (0x0)
mem_wb.mem_readdata                        0 (0x0)
mem_wb.instruction                         0 (0x0)
mem_wb.alu_result                          0 (0x0)
mem_wb.sextImm                             0 (0x0)
mem_wb.alu_result (input)                  1234 (0x4d2)
mem_wb.mem_readdata (input)                0 (0x0)
mem_wb.sextImm (input)                     0 (0x0)
mem_wb.instruction (input)                 230067 (0x382b3)
mem_wb_ctrl.wb_ctrl_writeback_src          0 (0x0)
mem_wb_ctrl.wb_ctrl_writeback_src (input)1 (0x1)
```

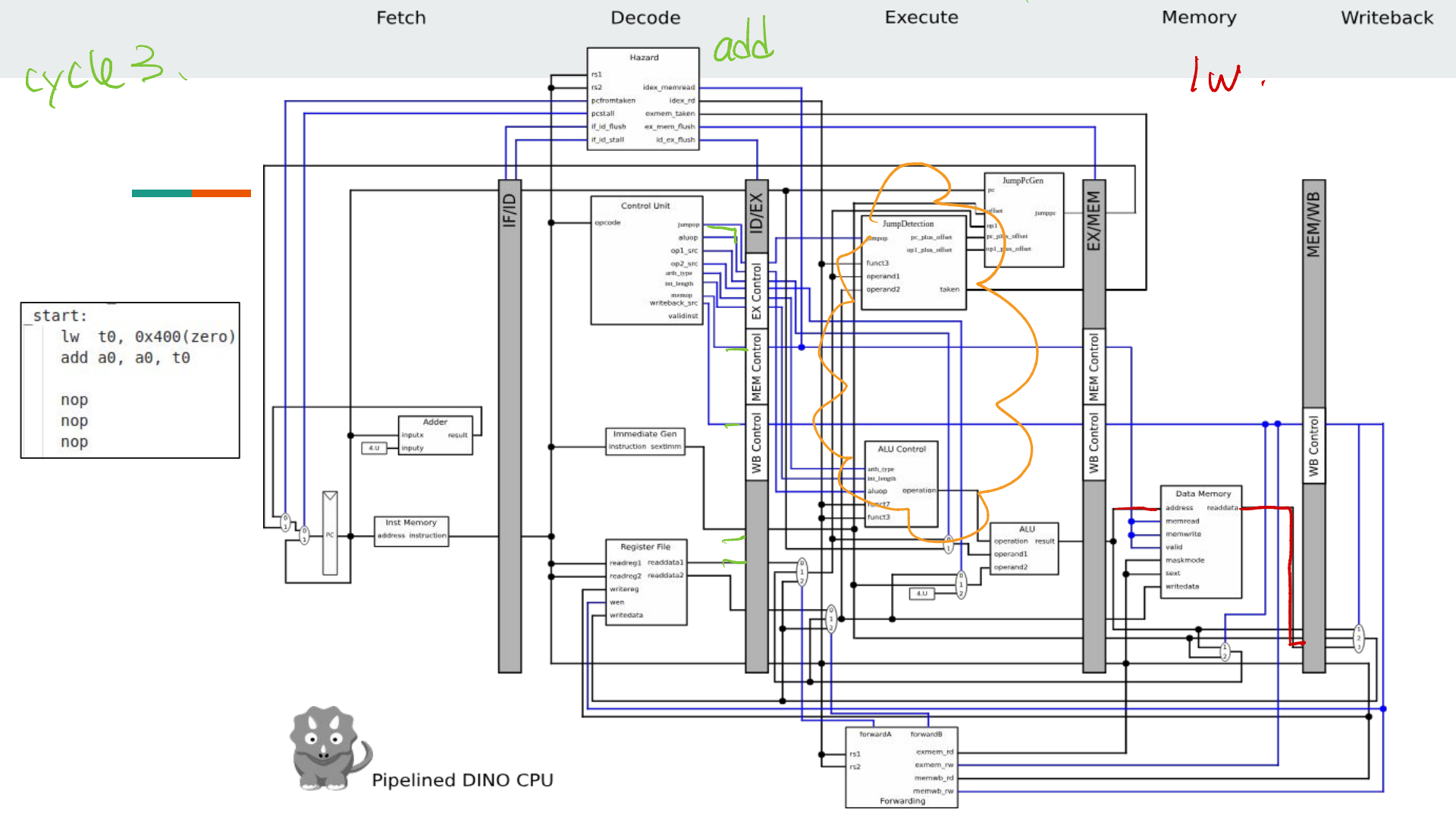
lwfwd

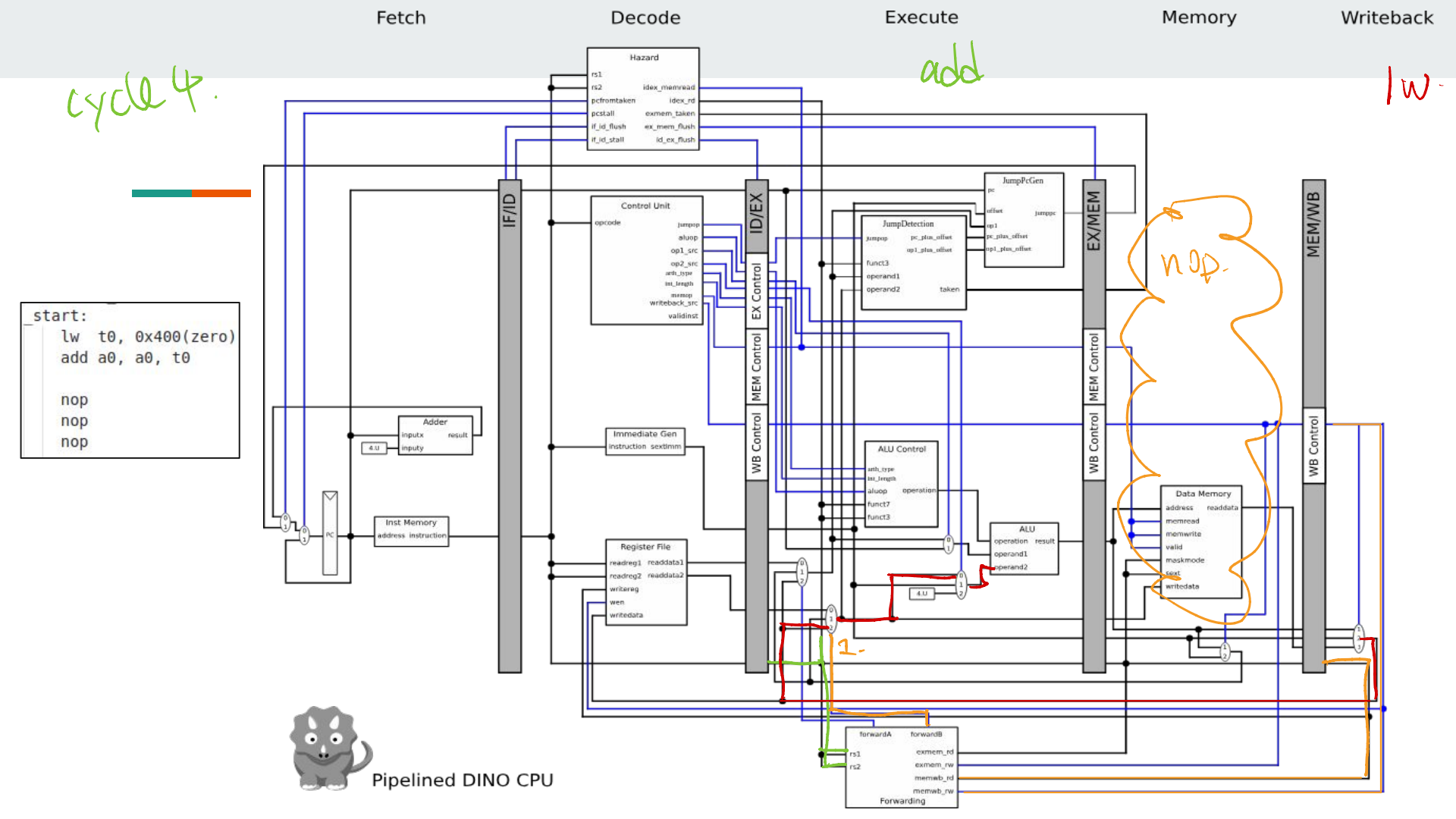
```
_start:
    lw  t0, 0x400(zero) # (reg[5] = mem[0x100])
    add a0, a0, t0      # (reg[10] = reg[10] + reg[5])

    nop
    nop
    nop
```




Fetch
Decode
Execute
Memory
Writeback
cycle 2.
if load
if rs1 or rs2
== rd
add.
if load.
lw
inst(11,7).
true.
_start:
lw t0, 0x400(zero)
add a0, a0, t0
nop
nop
nop
Hazard
rs1
rs2
pcfromtaken
pcstall
if_id_flush
if_id_stall
idex_memread
idex_rd
exmem_taken
ex_mem_flush
id_ex_flush
IF/ID
ID/EX
EX/MEM
MEM/WB
Control Unit
opcode
jumpop
aluop
op1_src
op2_src
arth_type
ins_length
memop
writeback_src
validinst
EX Control
MEM Control
WB Control
JumpPcGen
pc
offset
jumppc
op1
pc_plus_offset
op1_plus_offset
JumpDetection
jumpop
funct3
operand1
operand2
taken
Adder
inputx
inputy
result
4.U
Immediate Gen
instruction
sextImm
Inst Memory
address
instruction
pc
Register File
readreg1
readreg2
writereg
wen
writedata
readdata1
readdata2
ALU Control
operation
funct7
funct3
ALU
operation
result
operand1
operand2
Data Memory
address
readdata
memread
memwrite
valid
maskmode
sext
writedata
forwardA
forwardB
rs1
rs2
exmem_rd
exmem_rw
memwb_rd
memwb_rw
Forwarding
Pipelined DINO CPU


Fetch
Decode
Execute
Memory
Writeback
cycle 3.
add
lw.
_start:
lw t0, 0x400(zero)
add a0, a0, t0
nop
nop
nop
Hazard
IF/ID
ID/EX
EX/MEM
MEM/WB
Control Unit
JumpPcGen
JumpDetection
EX Control
MEM Control
WB Control
Adder
Immediate Gen
ALU Control
Data Memory
Inst Memory
Register File
ALU
Forwarding
Pipelined DINO CPU


Fetch
Decode
Execute
Memory
Writeback
cycle 4.
add
lw
nop
1-
_start:
lw t0, 0x400(zero)
add a0, a0, t0
nop
nop
nop
Hazard
rs1
rs2
pcfromtaken
pcstall
if_id_flush
if_id_stall
idex_memread
idex_rd
exmem_taken
ex_mem_flush
id_ex_flush
IF/ID
ID/EX
EX/MEM
MEM/WB
Control Unit
opcode
jumpop
aluop
op1_src
op2_src
arth_type
ins_length
memop
writeback_src
validinst
EX Control
MEM Control
WB Control
JumpPcGen
pc
offset
jumppc
op1
pc_plus_offset
op1_plus_offset
JumpDetection
jumpop
funct3
operand1
operand2
taken
Adder
inputx
inputy
result
4.U
Immediate Gen
instruction
sextImm
Inst Memory
address
instruction
PC
Register File
readreg1
readreg2
writereg
wen
writedata
readdata1
readdata2
ALU Control
operation
funct7
funct3
ALU
operation
result
operand1
operand2
Data Memory
address
readdata
memread
memwrite
valid
maskmode
sext
writedata
forwardA
forwardB
exmem_rd
exmem_rw
memwb_rd
memwb_rw
Forwarding
Pipelined DINO CPU

Cycle 2

```
hazard.io.id_ex_flush          1 (0x1)
hazard.io.rs2                  5 (0x5)
hazard.io.exmem_taken          0 (0x0)
hazard.io.ex_mem_flush         0 (0x0)
hazard.io.idex_memread         1 (0x1)
hazard.io.rs1                  10 (0xa)
hazard.io.if_id_flush          0 (0x0)
hazard.io.pcstall              1 (0x1)
hazard.io.idex_rd              5 (0x5)
hazard.io.if_id_stall          1 (0x1)
hazard.io.pcfromtaken          0 (0x0)
```

```
control.io.memop               0 (0x0)
control.io.op2_src             0 (0x0)
control.io.op1_src             0 (0x0)
control.io.jumpop              0 (0x0)
control.io.aluop               1 (0x1)
control.io.int_length          0 (0x0)
control.io.arth_type           0 (0x0)
control.io.writeback_src       1 (0x1)
control.io.opcode              51 (0x33)
registers.io.readdata1         5 (0x5)
registers.io.readdata2         4294967295 (0xffffffff)
registers.io.readreg1          10 (0xa)
registers.io.writereg          0 (0x0)
registers.io.readreg2          5 (0x5)
registers.io.writedata         0 (0x0)
registers.io.wen               0 (0x0)
immGen.io.instruction          5571891 (0x550533)
immGen.io.sextImm              0 (0x0)
aluControl.io.int_length       0 (0x0)
aluControl.io.funct3           2 (0x2)
aluControl.io.arth_type        0 (0x0)
aluControl.io.aluop            2 (0x2)
aluControl.io.funct7           32 (0x20)
aluControl.io.operation        0 (0x0)
alu.io.operand1                0 (0x0)
alu.io.result                  1024 (0x400)
alu.io.operand2                1024 (0x400)
alu.io.operation               0 (0x0)
```

```
if_id.pc                                  4 (0x4)
if_id.instruction                         5571891 (0x550533)
if_id.instruction (input)                 5571891 (0x550533)
if_id.pc (input)                          4 (0x4)
id_ex.instruction                         1073750659 (0x40002283)
id_ex.readdata2                           0 (0x0)
id_ex.pc                                  0 (0x0)
id_ex.readdata1                           0 (0x0)
id_ex.sextImm                             1024 (0x400)
id_ex.instruction (input)                 0 (0x0)
id_ex.pc (input)                          0 (0x0)
id_ex.readdata1 (input)                   0 (0x0)
id_ex.sextImm (input)                     0 (0x0)
id_ex.readdata2 (input)                   0 (0x0)
id_ex_ctrl.ex_ctrl_arth_type              0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src                1 (0x1)
id_ex_ctrl.mem_ctrl_memop                 1 (0x1)
id_ex_ctrl.ex_ctrl_aluop                  2 (0x2)
id_ex_ctrl.ex_ctrl_jumpop                 0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src          3 (0x3)
id_ex_ctrl.ex_ctrl_int_length             0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src                0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src (input)        0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src (input)  0 (0x0)
id_ex_ctrl.ex_ctrl_arth_type (input)      0 (0x0)
id_ex_ctrl.ex_ctrl_aluop (input)          0 (0x0)
id_ex_ctrl.ex_ctrl_jumpop (input)         0 (0x0)
id_ex_ctrl.ex_ctrl_int_length (input)     0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src (input)        0 (0x0)
id_ex_ctrl.mem_ctrl_memop (input)         0 (0x0)
ex_mem.alu_result                         0 (0x0)
ex_mem.mem_writedata                      0 (0x0)
ex_mem.sextImm                            0 (0x0)
ex_mem.taken                              0 (0x0)
ex_mem.jumppc                             0 (0x0)
ex_mem.instruction                        0 (0x0)
ex_mem.sextImm (input)                    1024 (0x400)
ex_mem.instruction (input)                1073750659 (0x40002283)
ex_mem.taken (input)                      0 (0x0)
ex_mem.alu_result (input)                 1024 (0x400)
ex_mem.jumppc (input)                     0 (0x0)
ex_mem.mem_writedata (input)              0 (0x0)
ex_mem_ctrl.mem_ctrl_memop                0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src         0 (0x0)
ex_mem_ctrl.mem_ctrl_memop (input)        1 (0x1)
ex_mem_ctrl.wb_ctrl_writeback_src (input) 3 (0x3)
```

Cycle 3

```
if_id.pc                                4 (0x4)
if_id.instruction                       5571891 (0x550533)
if_id.instruction (input)               19 (0x13)
if_id.pc (input)                        8 (0x8)
id_ex.instruction                       0 (0x0)
id_ex.readdata2                         0 (0x0)
id_ex.pc                                0 (0x0)
id_ex.readdata1                         0 (0x0)
id_ex.sextImm                           0 (0x0)
id_ex.instruction (input)               5571891 (0x550533)
id_ex.pc (input)                        4 (0x4)
id_ex.readdata1 (input)                 5 (0x5)
id_ex.sextImm (input)                   0 (0x0)
id_ex.readdata2 (input)                 4294967295 (0xffffffff)
id_ex_ctrl.ex_ctrl_arth_type            0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src              0 (0x0)
id_ex_ctrl.mem_ctrl_memop               0 (0x0)
id_ex_ctrl.ex_ctrl_aluop                0 (0x0)
id_ex_ctrl.ex_ctrl_jumpop               0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src        0 (0x0)
id_ex_ctrl.ex_ctrl_int_length           0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src              0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src (input)      0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src (input)1 (0x1)
id_ex_ctrl.ex_ctrl_arth_type (input)    0 (0x0)
id_ex_ctrl.ex_ctrl_aluop (input)        1 (0x1)
id_ex_ctrl.ex_ctrl_jumpop (input)       0 (0x0)
id_ex_ctrl.ex_ctrl_int_length (input)   0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src (input)      0 (0x0)
id_ex_ctrl.mem_ctrl_memop (input)       0 (0x0)
ex_mem.alu_result                       1024 (0x400)
ex_mem.mem_writedata                    0 (0x0)
ex_mem.sextImm                          1024 (0x400)
ex_mem.taken                            0 (0x0)
ex_mem.jumppc                           0 (0x0)
ex_mem.instruction                      1073750659 (0x40002283)
ex_mem.sextImm (input)                  0 (0x0)
ex_mem.instruction (input)              0 (0x0)
ex_mem.taken (input)                    0 (0x0)
ex_mem.alu_result (input)               0 (0x0)
ex_mem.jumppc (input)                   0 (0x0)
ex_mem.mem_writedata (input)            0 (0x0)
ex_mem_ctrl.mem_ctrl_memop              1 (0x1)
ex_mem_ctrl.wb_ctrl_writeback_src       3 (0x3)
ex_mem_ctrl.mem_ctrl_memop (input)      0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src (input)0 (0x0)
```

```
mem_wb.mem_readdata                     0 (0x0)
mem_wb.instruction                      0 (0x0)
mem_wb.alu_result                       0 (0x0)
mem_wb.sextImm                          0 (0x0)
mem_wb.alu_result (input)               1024 (0x400)
mem_wb.mem_readdata (input)             1 (0x1)
mem_wb.sextImm (input)                  1024 (0x400)
mem_wb.instruction (input)              1073750659 (0x40002283)
mem_wb_ctrl.wb_ctrl_writeback_src       0 (0x0)
mem_wb_ctrl.wb_ctrl_writeback_src (input)3 (0x3)
```

```
Single stepper> dump dmem
dmem.valid                      1 (0x1)
dmem.readdata                   1 (0x1)
dmem.memread                    1 (0x1)
dmem.good                       1 (0x1)
dmem.maskmode                   2 (0x2)
dmem.sext                       1 (0x1)
dmem.address                    1024 (0x400)
dmem.memwrite                   0 (0x0)
dmem.writedata                  0 (0x0)
Single stepper> dump alu
alu.io.operand1                 0 (0x0)
alu.io.result                   0 (0x0)
alu.io.operand2                 0 (0x0)
alu.io.operation                31 (0x1f)
Single stepper> dump registers
registers.io.readdata1          5 (0x5)
registers.io.readdata2          4294967295 (0xffffffff)
registers.io.readreg1           10 (0xa)
registers.io.writereg           0 (0x0)
registers.io.readreg2           5 (0x5)
registers.io.writedata          0 (0x0)
registers.io.wen                0 (0x0)
```

Cycle 4

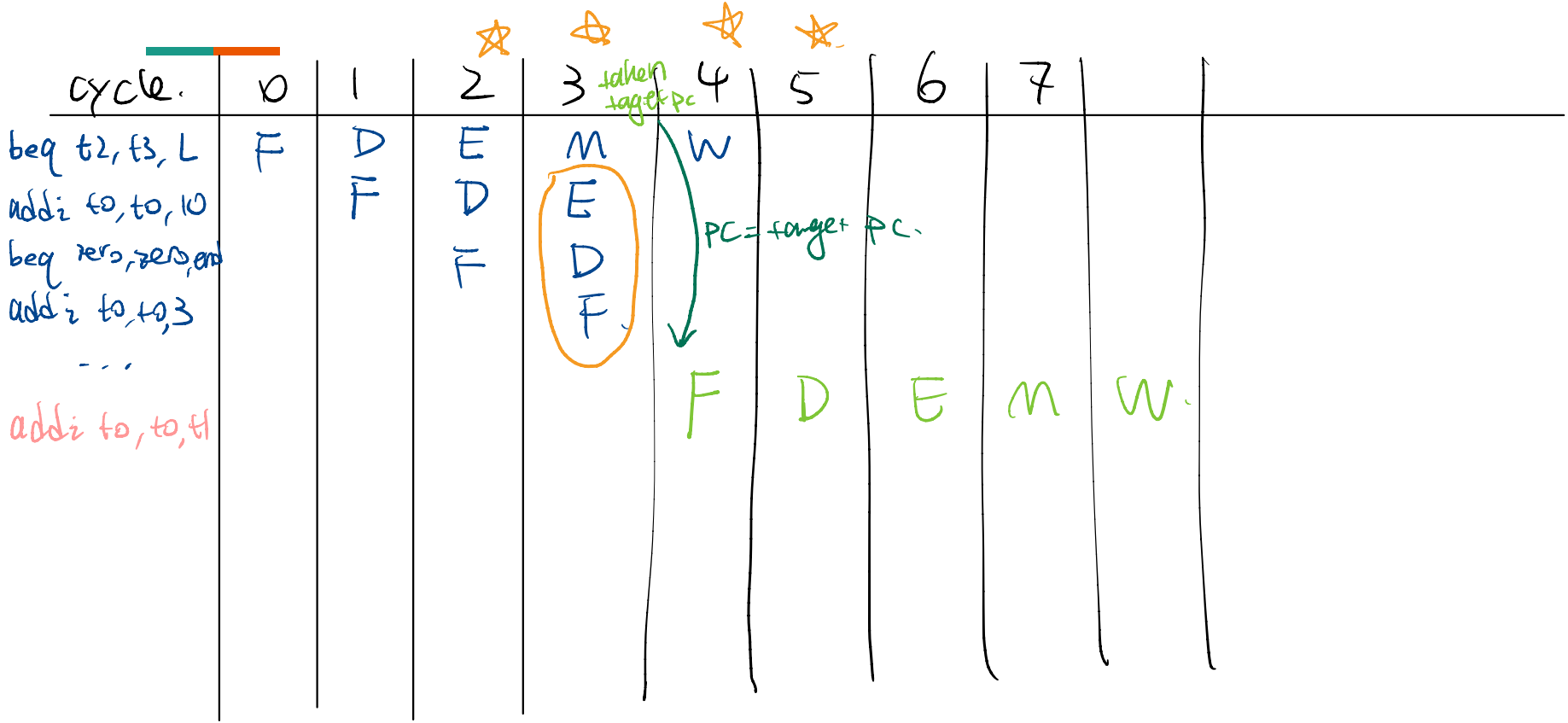
```
Single stepper> dump alu
alu.io.operand1                 5 (0x5)
alu.io.result                   6 (0x6)
alu.io.operand2                 1 (0x1)
alu.io.operation                0 (0x0)
Single stepper> dump forwarding
forwarding.io.memwbrd           5 (0x5)
forwarding.io.memwbrw           1 (0x1)
forwarding.io.forwardB          2 (0x2)
forwarding.io.forwardA          0 (0x0)
forwarding.io.exmemrd           0 (0x0)
forwarding.io.rs1               10 (0xa)
forwarding.io.rs2               5 (0x5)
forwarding.io.exmemrw           0 (0x0)
Single stepper> dump hazard
hazard.io.id_ex_flush           0 (0x0)
hazard.io.rs2                   0 (0x0)
hazard.io.exmem_taken           0 (0x0)
hazard.io.ex_mem_flush          0 (0x0)
hazard.io.idex_memread          0 (0x0)
hazard.io.rs1                   0 (0x0)
hazard.io.if_id_flush           0 (0x0)
hazard.io.pcstall               0 (0x0)
hazard.io.idex_rd               10 (0xa)
hazard.io.if_id_stall           0 (0x0)
hazard.io.pcfromtaken           0 (0x0)
Single stepper> dump registers
registers.io.readdata1          0 (0x0)
registers.io.readdata2          0 (0x0)
registers.io.readreg1           0 (0x0)
registers.io.writereg           5 (0x5)
registers.io.readreg2           0 (0x0)
registers.io.writedata          1 (0x1)
registers.io.wen                1 (0x1)
```

wb stage

beq-True

```
_start:
    beq t2, t3, label   # if reg[7] == reg[28], go to label.
    addi t0, t0, 10  # else reg[5] = reg[5] + 10
    beq zero, zero, end # no matter what, go to end
    addi t0, t0, 3 # reg[5] = reg[5] + 10; this line should never be executed
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
label:
    add t0, t0, t1     # reg[5] = reg[5] + reg[6]

end:
    nop
```


cycle
0
1
2
3
4
5
6
7
taken target pc
beq t2, t3, L
addi t0, t0, 10
beq zero, zero, end
addi t0, t0, 3
...
addi t0, t0, t1
F
D
E
M
W
F
D
E
M
W
F
D
E
M
W
F
D
E
M
W
PC = target PC.

beq zero.

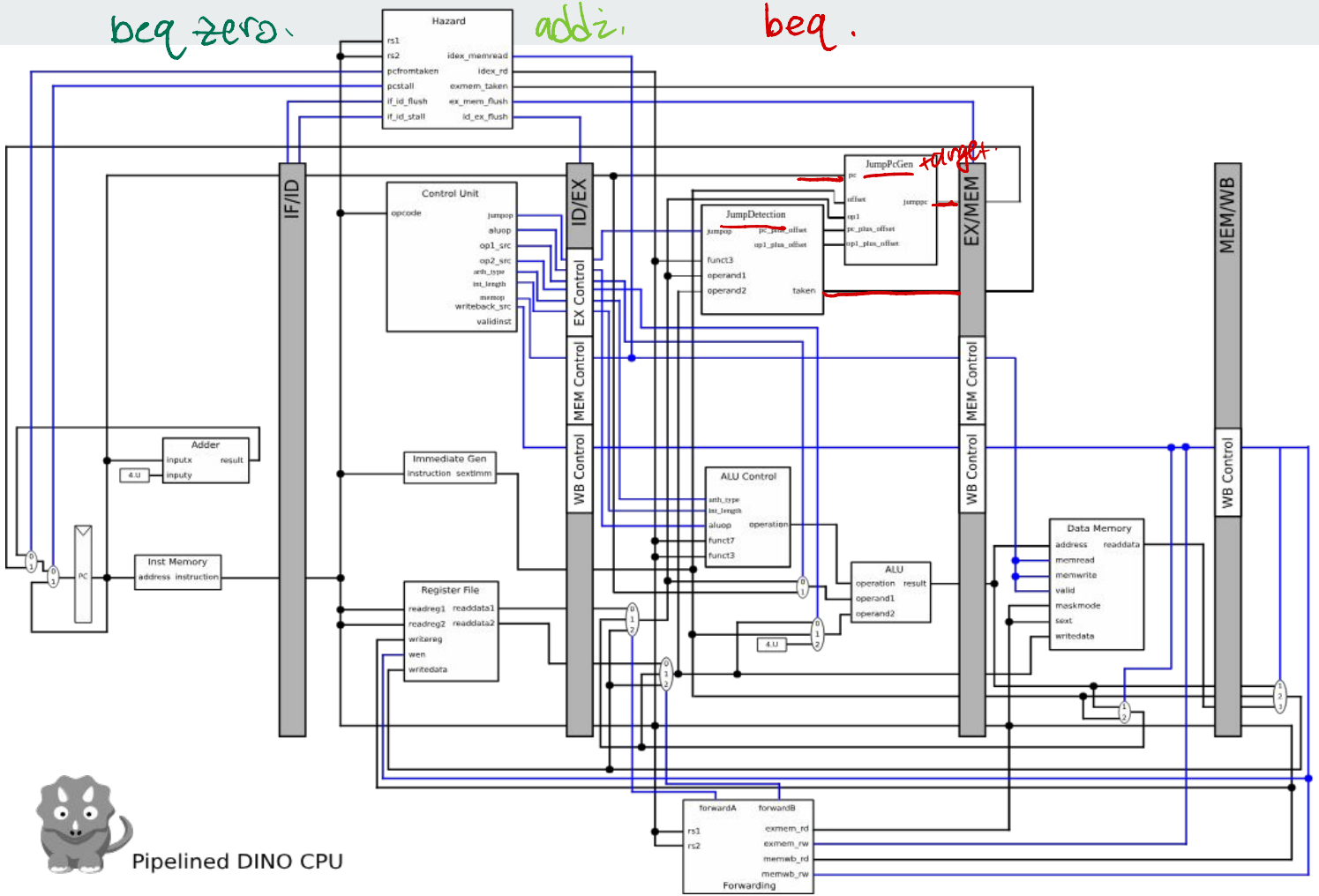
addi.

beq.

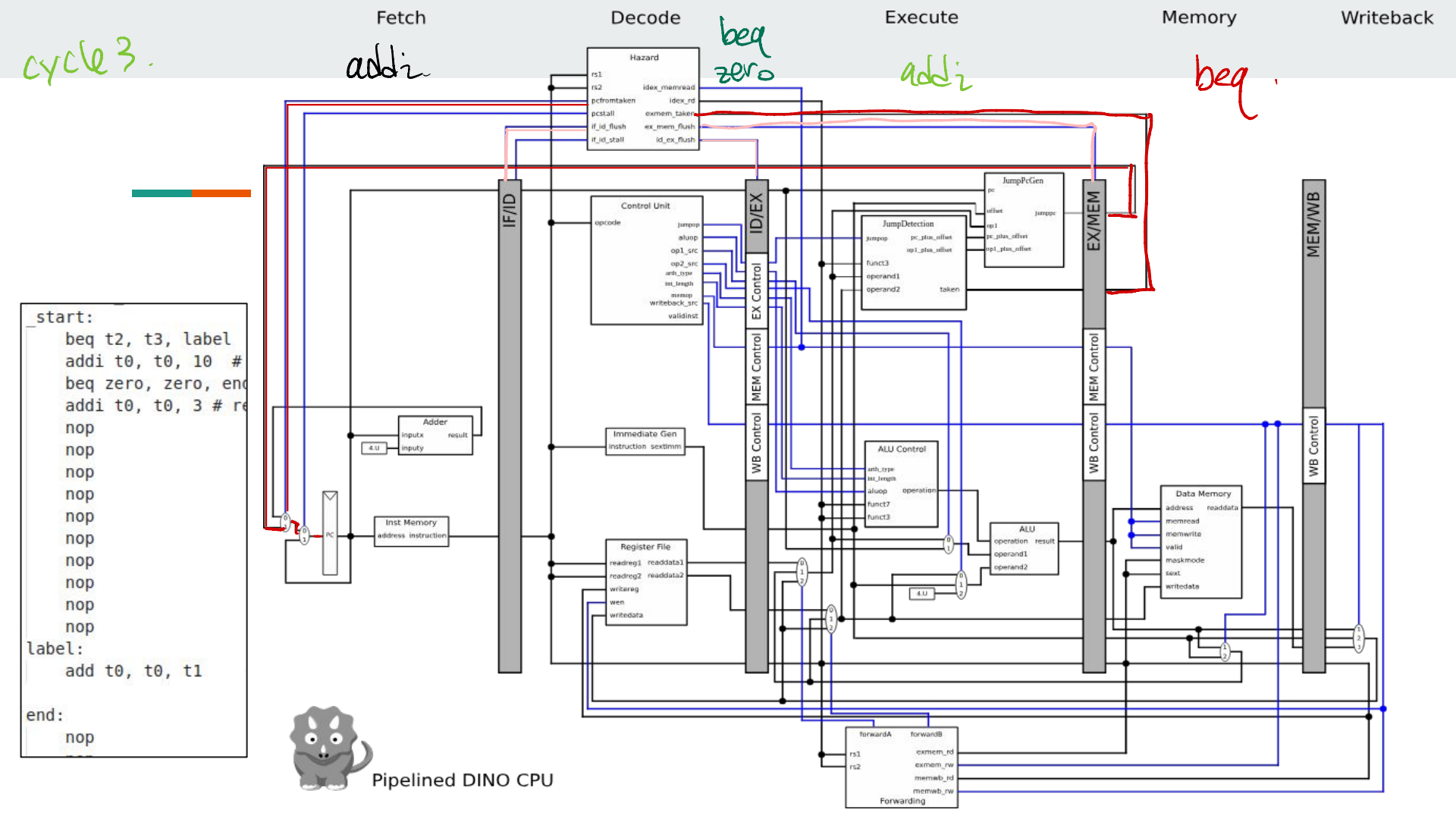
cycle 2.

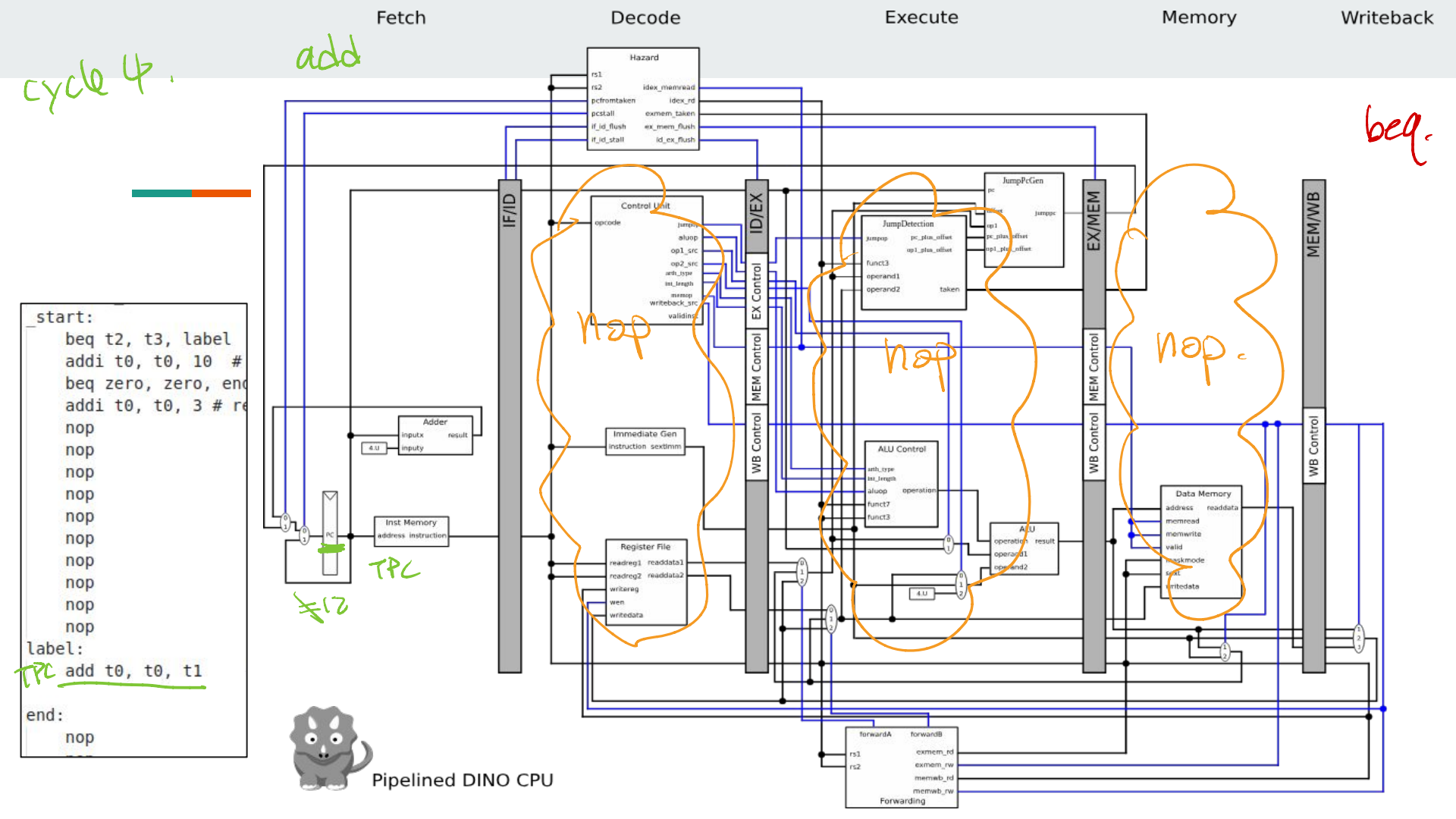
```
_start:
    beq t2, t3, label
    addi t0, t0, 10  #
    beq zero, zero, end
    addi t0, t0, 3 # re
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
label:
    add t0, t0, t1

end:
    nop
```



Pipelined DINO CPU

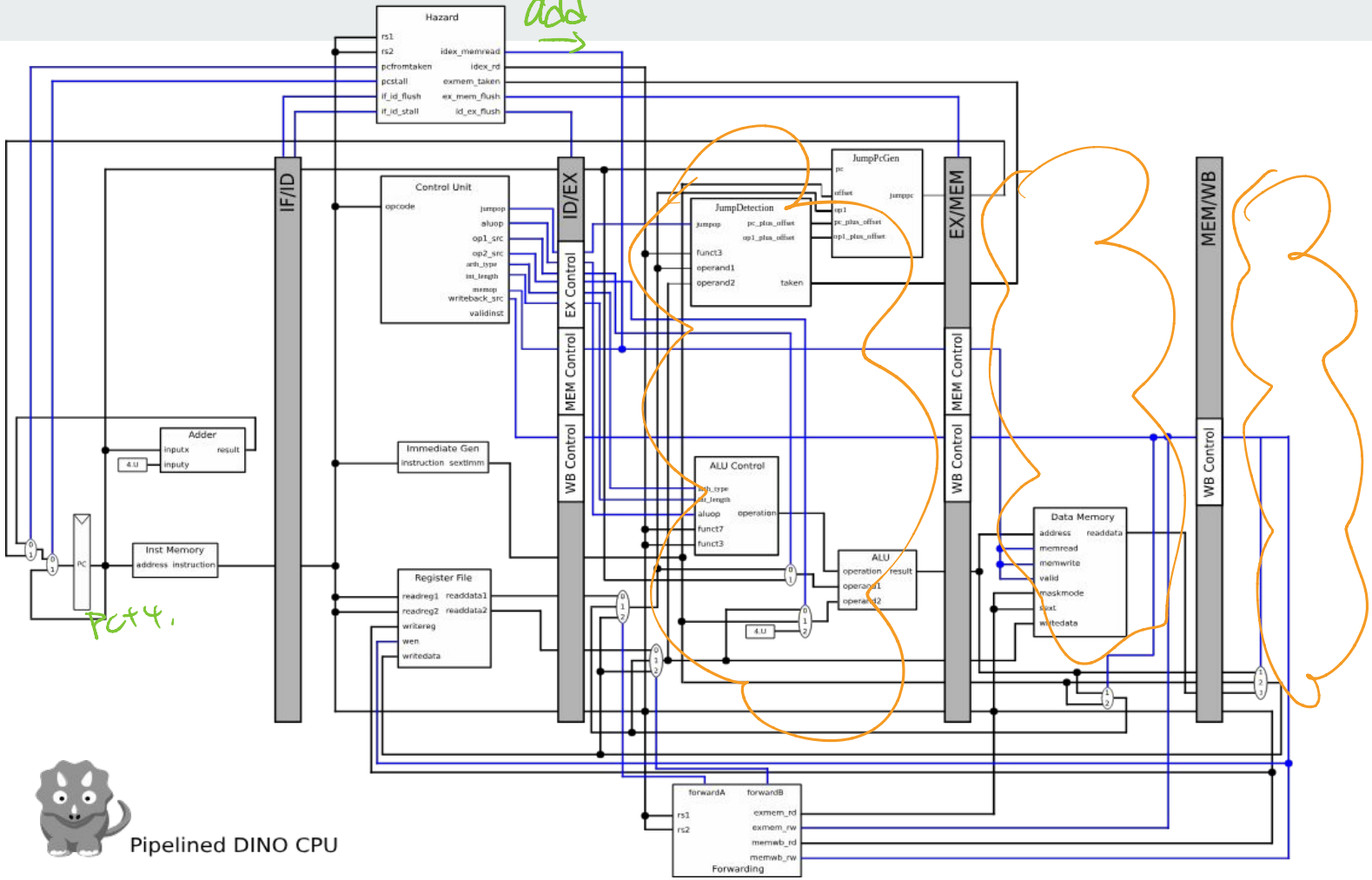

Fetch
Decode
Execute
Memory
Writeback
cycle 3.
addi
beq zero
addi
beq
_start:
beq t2, t3, label
addi t0, t0, 10 #
beq zero, zero, end
addi t0, t0, 3 # re
nop
nop
nop
nop
nop
nop
nop
nop
nop
nop
nop
label:
add t0, t0, t1
end:
nop
Hazard
rs1
rs2
pcfromtaken
pcstall
if_id_flush
if_id_stall
idex_memread
idex_rd
exmem_taken
ex_mem_flush
id_ex_flush
IF/ID
ID/EX
EX/MEM
MEM/WB
Control Unit
opcode
jumpop
aluop
op1_src
op2_src
arth_type
ins_length
memop
writeback_src
validinst
EX Control
MEM Control
WB Control
JumpPcGen
pc
offset
jumppc
op1
pc_plus_offset
op1_plus_offset
JumpDetection
jumpop
funct3
operand1
operand2
taken
Adder
inputx
inputy
result
4.U
Inst Memory
address
instruction
PC
Immediate Gen
instruction
sextImm
Register File
readreg1
readreg2
writereg
wen
writedata
readdata1
readdata2
ALU Control
arth_type
ins_length
aluop
funct7
funct3
operation
ALU
operation
result
operand1
operand2
Data Memory
address
memread
memwrite
valid
maskmode
sext
writedata
readdata
forwardA
forwardB
rs1
rs2
exmem_rd
exmem_rw
memwb_rd
memwb_rw
Forwarding
Pipelined DINO CPU


Fetch
Decode
Execute
Memory
Writeback
cycle 4.
add
beq.
nop
nop
nop.
TPC
+12
TPC
_start:
beq t2, t3, label
addi t0, t0, 10 #
beq zero, zero, end
addi t0, t0, 3 # re
nop
nop
nop
nop
nop
nop
nop
nop
nop
nop
label:
add t0, t0, t1
end:
nop
Hazard
IF/ID
ID/EX
EX/MEM
MEM/WB
Control Unit
JumpPcGen
JumpDetection
Adder
Immediate Gen
ALU Control
ALU
Inst Memory
Register File
Data Memory
EX Control
MEM Control
WB Control
Forwarding
Pipelined DINO CPU

cycle 5.

```
_start:
    beq t2, t3, label
    addi t0, t0, 10  #
    beq zero, zero, end
    addi t0, t0, 3 # re
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
label:
    add t0, t0, t1

end:
    nop
```



Pipelined DINO CPU

Cycle 2

```
Single stepper> dump hazard
hazard.io.id_ex_flush          0 (0x0)
hazard.io.rs2                  10 (0xa)
hazard.io.exmem_taken          0 (0x0)
hazard.io.ex_mem_flush         0 (0x0)
hazard.io.idex_memread         0 (0x0)
hazard.io.rs1                  5 (0x5)
hazard.io.if_id_flush          0 (0x0)
hazard.io.pcstall              0 (0x0)
hazard.io.idex_rd              24 (0x18)
hazard.io.if_id_stall          0 (0x0)
hazard.io.pcfromtaken          0 (0x0)
```

Ex

beq

```
if_id.pc                                4 (0x4)
if_id.instruction                       10650259 (0xa28293)
if_id.instruction (input)               33557091 (0x2000a63)
if_id.pc (input)                        8 (0x8)
id_ex.instruction                       63147107 (0x3c38c63)
id_ex.readdata2                         5678 (0x162e)
id_ex.pc                                0 (0x0)
id_ex.readdata1                         5678 (0x162e)
id_ex.sextImm                           56 (0x38)
id_ex.instruction (input)               10650259 (0xa28293)
id_ex.pc (input)                        4 (0x4)
id_ex.readdata1 (input)                 1234 (0x4d2)
id_ex.sextImm (input)                   10 (0xa)
id_ex.readdata2 (input)                 0 (0x0)
id_ex_ctrl.ex_ctrl_arth_type            0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src              0 (0x0)
id_ex_ctrl.mem_ctrl_memop               0 (0x0)
id_ex_ctrl.ex_ctrl_aluop                0 (0x0)
id_ex_ctrl.ex_ctrl_jumpop               3 (0x3)
id_ex_ctrl.wb_ctrl_writeback_src        0 (0x0)
id_ex_ctrl.ex_ctrl_int_length           0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src              0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src (input)      0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src (input)1 (0x1)
id_ex_ctrl.ex_ctrl_arth_type (input)    1 (0x1)
id_ex_ctrl.ex_ctrl_aluop (input)        1 (0x1)
id_ex_ctrl.ex_ctrl_jumpop (input)       0 (0x0)
id_ex_ctrl.ex_ctrl_int_length (input)   0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src (input)      1 (0x1)
id_ex_ctrl.mem_ctrl_memop (input)       0 (0x0)
```

```
ex_mem.alu_result                       0 (0x0)
ex_mem.mem_writedata                    0 (0x0)
ex_mem.sextImm                          0 (0x0)
ex_mem.taken                            0 (0x0)
ex_mem.jumppc                           0 (0x0)
ex_mem.instruction                      0 (0x0)
ex_mem.sextImm (input)                  56 (0x38)
ex_mem.instruction (input)              63147107 (0x3c38c63)
ex_mem.taken (input)                    1 (0x1)
ex_mem.alu_result (input)               0 (0x0)
ex_mem.jumppc (input)                   56 (0x38)
ex_mem.mem_writedata (input)            5678 (0x162e)
ex_mem_ctrl.mem_ctrl_memop              0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src       0 (0x0)
ex_mem_ctrl.mem_ctrl_memop (input)      0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src (input)0 (0x0)
```

Cycle 3

```
Single stepper> dump hazard
hazard.io.id_ex_flush          1 (0x1)
hazard.io.rs2                  0 (0x0)
hazard.io.exmem_taken          1 (0x1)
hazard.io.ex_mem_flush         1 (0x1)
hazard.io.idex_memread         0 (0x0)
hazard.io.rs1                  0 (0x0)
hazard.io.if_id_flush          1 (0x1)
hazard.io.pcstall              0 (0x0)
hazard.io.idex_rd              5 (0x5)
hazard.io.if_id_stall          0 (0x0)
hazard.io.pcfromtaken          1 (0x1)
```

MEM

beq

```
if_id.pc                                  8 (0x8)
if_id.instruction                         33557091 (0x2000a63)
if_id.instruction (input)                 0 (0x0)
if_id.pc (input)                          0 (0x0)
id_ex.instruction                         10650259 (0xa28293)
id_ex.readdata2                           0 (0x0)
id_ex.pc                                  4 (0x4)
id_ex.readdata1                           1234 (0x4d2)
id_ex.sextImm                             10 (0xa)
id_ex.instruction (input)                 0 (0x0)
id_ex.pc (input)                          0 (0x0)
id_ex.readdata1 (input)                   0 (0x0)
id_ex.sextImm (input)                     0 (0x0)
id_ex.readdata2 (input)                   0 (0x0)
id_ex_ctrl.ex_ctrl_arth_type              1 (0x1)
id_ex_ctrl.ex_ctrl_op2_src                1 (0x1)
id_ex_ctrl.mem_ctrl_memop                 0 (0x0)
id_ex_ctrl.ex_ctrl_aluop                  1 (0x1)
id_ex_ctrl.ex_ctrl_jumpop                 0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src          1 (0x1)
id_ex_ctrl.ex_ctrl_int_length             0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src                0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src (input)        0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src (input)  0 (0x0)
id_ex_ctrl.ex_ctrl_arth_type (input)      0 (0x0)
id_ex_ctrl.ex_ctrl_aluop (input)          0 (0x0)
id_ex_ctrl.ex_ctrl_jumpop (input)         0 (0x0)
id_ex_ctrl.ex_ctrl_int_length (input)     0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src (input)        0 (0x0)
id_ex_ctrl.mem_ctrl_memop (input)         0 (0x0)
```

```
ex_mem.alu_result                         0 (0x0)
ex_mem.mem_writedata                      5678 (0x162e)
ex_mem.sextImm                            56 (0x38)
ex_mem.taken                              1 (0x1)
ex_mem.jumppc                             56 (0x38)
ex_mem.instruction                        63147107 (0x3c38c63)
ex_mem.sextImm (input)                    0 (0x0)
ex_mem.instruction (input)                0 (0x0)
ex_mem.taken (input)                      0 (0x0)
ex_mem.alu_result (input)                 0 (0x0)
ex_mem.jumppc (input)                     0 (0x0)
ex_mem.mem_writedata (input)              0 (0x0)
ex_mem_ctrl.mem_ctrl_memop                0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src         0 (0x0)
ex_mem_ctrl.mem_ctrl_memop (input)        0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src (input)0 (0x0)
mem_wb.mem_readdata                       0 (0x0)
mem_wb.instruction                        0 (0x0)
mem_wb.alu_result                         0 (0x0)
mem_wb.sextImm                            0 (0x0)
mem_wb.alu_result (input)                 0 (0x0)
mem_wb.mem_readdata (input)               0 (0x0)
mem_wb.sextImm (input)                    56 (0x38)
mem_wb.instruction (input)                63147107 (0x3c38c63)
mem_wb_ctrl.wb_ctrl_writeback_src         0 (0x0)
mem_wb_ctrl.wb_ctrl_writeback_src (input)0 (0x0)
```

Cycle 4

```
Single stepper> print piperegs
if_id.pc                                0 (0x0)
if_id.instruction                       0 (0x0)
if_id.instruction (input)               6455987 (0x6282b3)
if_id.pc (input)                        56 (0x38)
id_ex.instruction                       0 (0x0)
id_ex.readdata2                         0 (0x0)
id_ex.pc                                0 (0x0)
id_ex.readdata1                         0 (0x0)
id_ex.sextImm                           0 (0x0)
id_ex.instruction (input)               0 (0x0)
id_ex.pc (input)                        0 (0x0)
id_ex.readdata1 (input)                 0 (0x0)
id_ex.sextImm (input)                   0 (0x0)
id_ex.readdata2 (input)                 0 (0x0)
id_ex_ctrl.ex_ctrl_arth_type            0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src              0 (0x0)
id_ex_ctrl.mem_ctrl_memop               0 (0x0)
id_ex_ctrl.ex_ctrl_aluop                0 (0x0)
id_ex_ctrl.ex_ctrl_jumpop               0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src        0 (0x0)
id_ex_ctrl.ex_ctrl_int_length           0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src              0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src (input)      0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src (input)0 (0x0)
id_ex_ctrl.ex_ctrl_arth_type (input)    0 (0x0)
id_ex_ctrl.ex_ctrl_aluop (input)        0 (0x0)
id_ex_ctrl.ex_ctrl_jumpop (input)       0 (0x0)
id_ex_ctrl.ex_ctrl_int_length (input)   0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src (input)      0 (0x0)
id_ex_ctrl.mem_ctrl_memop (input)       0 (0x0)
```

```
ex_mem.alu_result                       0 (0x0)
ex_mem.mem_writedata                    0 (0x0)
ex_mem.sextImm                          0 (0x0)
ex_mem.taken                            0 (0x0)
ex_mem.jumppc                           0 (0x0)
ex_mem.instruction                      0 (0x0)
ex_mem.sextImm (input)                  0 (0x0)
ex_mem.instruction (input)              0 (0x0)
ex_mem.taken (input)                    0 (0x0)
ex_mem.alu_result (input)               0 (0x0)
ex_mem.jumppc (input)                   0 (0x0)
ex_mem.mem_writedata (input)            0 (0x0)
ex_mem_ctrl.mem_ctrl_memop              0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src       0 (0x0)
ex_mem_ctrl.mem_ctrl_memop (input)      0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src (input)0 (0x0)
mem_wb.mem_readdata                     0 (0x0)
mem_wb.instruction                      63147107 (0x3c38c63)
mem_wb.alu_result                       0 (0x0)
mem_wb.sextImm                          56 (0x38)
mem_wb.alu_result (input)               0 (0x0)
mem_wb.mem_readdata (input)             0 (0x0)
mem_wb.sextImm (input)                  0 (0x0)
mem_wb.instruction (input)              0 (0x0)
mem_wb_ctrl.wb_ctrl_writeback_src       0 (0x0)
mem_wb_ctrl.wb_ctrl_writeback_src (input)0 (0x0)
```

nop

Cycle 5

```
Current cycle: 5
Single stepper> dump registers
registers.io.readdata1          1234 (0x4d2)
registers.io.readdata2          1 (0x1)
registers.io.readreg1           5 (0x5)
registers.io.writereg           0 (0x0)
registers.io.readreg2           6 (0x6)
registers.io.writedata          0 (0x0)
registers.io.wen                0 (0x0)
```

```
Single stepper> print piperegs
if_id.pc                                56 (0x38)
if_id.instruction                       6455987 (0x6282b3)
if_id.instruction (input)               19 (0x13)
if_id.pc (input)                        60 (0x3c)
id_ex.instruction                       0 (0x0)
id_ex.readdata2                         0 (0x0)
id_ex.pc                                0 (0x0)
id_ex.readdata1                         0 (0x0)
id_ex.sextImm                           0 (0x0)
id_ex.instruction (input)               6455987 (0x6282b3)
id_ex.pc (input)                        56 (0x38)
id_ex.readdata1 (input)                 1234 (0x4d2)
id_ex.sextImm (input)                   0 (0x0)
id_ex.readdata2 (input)                 1 (0x1)
id_ex_ctrl.ex_ctrl_arth_type            0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src              0 (0x0)
id_ex_ctrl.mem_ctrl_memop               0 (0x0)
id_ex_ctrl.ex_ctrl_aluop                0 (0x0)
id_ex_ctrl.ex_ctrl_jumpop               0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src        0 (0x0)
id_ex_ctrl.ex_ctrl_int_length           0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src              0 (0x0)
id_ex_ctrl.ex_ctrl_op1_src (input)      0 (0x0)
id_ex_ctrl.wb_ctrl_writeback_src (input)1 (0x1)
id_ex_ctrl.ex_ctrl_arth_type (input)    0 (0x0)
id_ex_ctrl.ex_ctrl_aluop (input)        1 (0x1)
id_ex_ctrl.ex_ctrl_jumpop (input)       0 (0x0)
id_ex_ctrl.ex_ctrl_int_length (input)   0 (0x0)
id_ex_ctrl.ex_ctrl_op2_src (input)      0 (0x0)
id_ex_ctrl.mem_ctrl_memop (input)       0 (0x0)
```

```
ex_mem.alu_result                       0 (0x0)
ex_mem.mem_writedata                    0 (0x0)
ex_mem.sextImm                          0 (0x0)
ex_mem.taken                            0 (0x0)
ex_mem.jumppc                           0 (0x0)
ex_mem.instruction                      0 (0x0)
ex_mem.sextImm (input)                  0 (0x0)
ex_mem.instruction (input)              0 (0x0)
ex_mem.taken (input)                    0 (0x0)
ex_mem.alu_result (input)               0 (0x0)
ex_mem.jumppc (input)                   0 (0x0)
ex_mem.mem_writedata (input)            0 (0x0)
ex_mem_ctrl.mem_ctrl_memop              0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src       0 (0x0)
ex_mem_ctrl.mem_ctrl_memop (input)      0 (0x0)
ex_mem_ctrl.wb_ctrl_writeback_src (input)0 (0x0)
mem_wb.mem_readdata                     0 (0x0)
mem_wb.instruction                      0 (0x0)
mem_wb.alu_result                       0 (0x0)
mem_wb.sextImm                          0 (0x0)
mem_wb.alu_result (input)               0 (0x0)
mem_wb.mem_readdata (input)             0 (0x0)
mem_wb.sextImm (input)                  0 (0x0)
mem_wb.instruction (input)              0 (0x0)
mem_wb_ctrl.wb_ctrl_writeback_src       0 (0x0)
mem_wb_ctrl.wb_ctrl_writeback_src (input)0 (0x0)
```

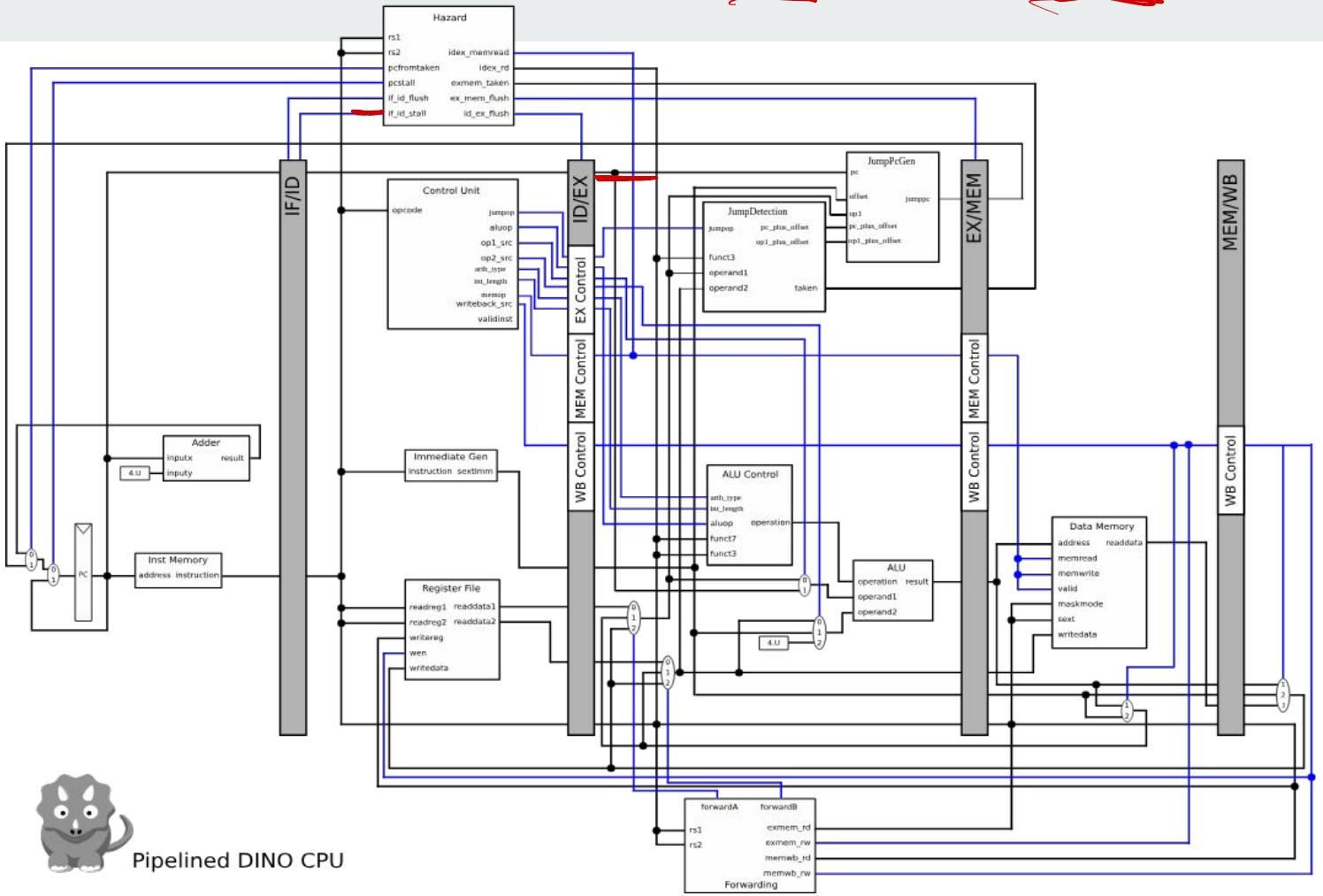
if_id.valid := ~hazard_io.if_id_stall

Fetch Decode Execute Memory Writeback

sd x5, 16(x5)

```
_start:
    beq t2, t3, label
    addi t0, t0, 10  #
    beq zero, zero, end
    addi t0, t0, 3 # re
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
label:
    add t0, t0, t1

end:
    nop
```



Pipelined DINO CPU