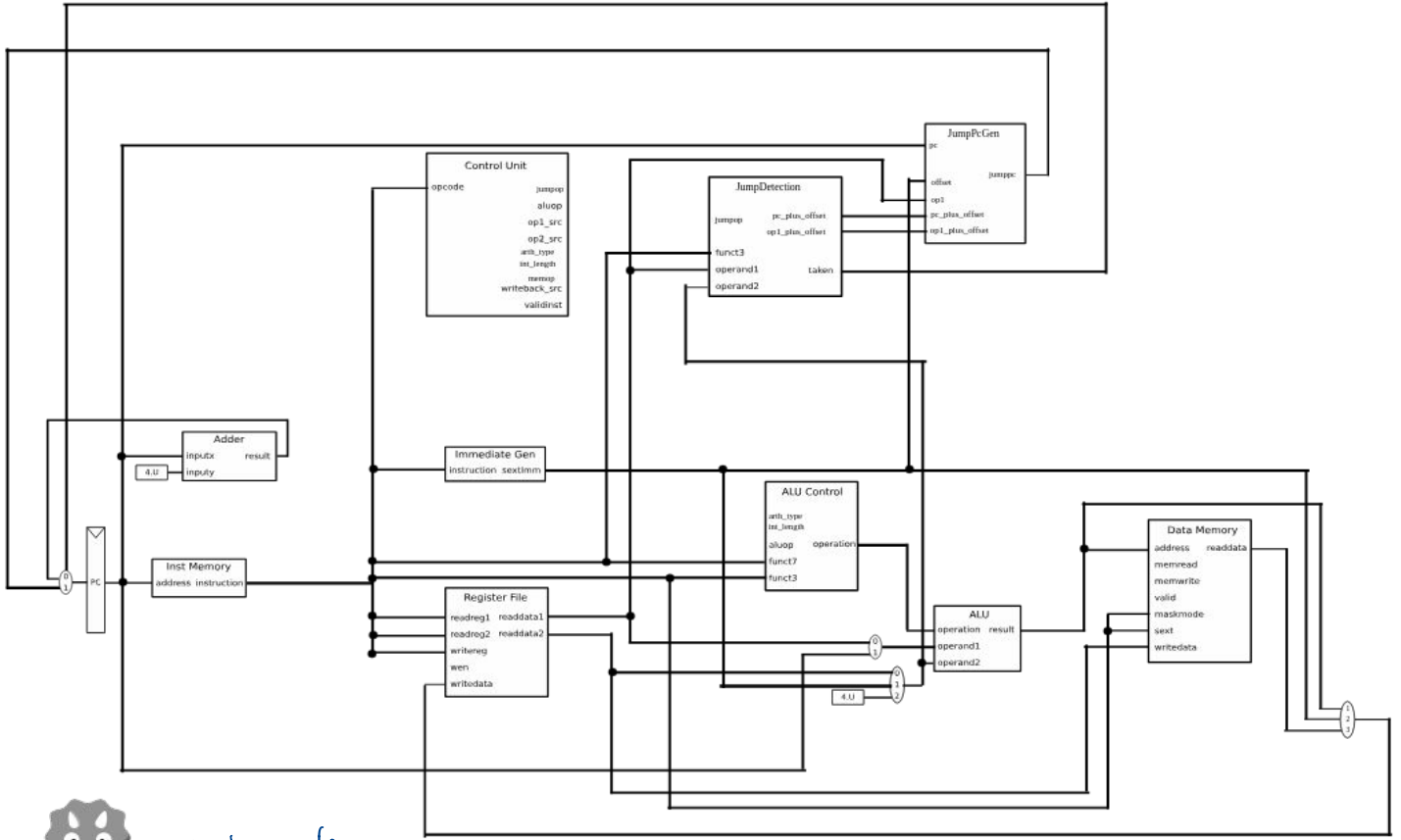
Discussion 4

Jan 30

Outline

1. DINOCPU assignment 3.1
2. Week 4 quiz



single cycle

~~Pipelined~~ DINO CPU

Fetch Decode Execute Memory Writeback

Hazard

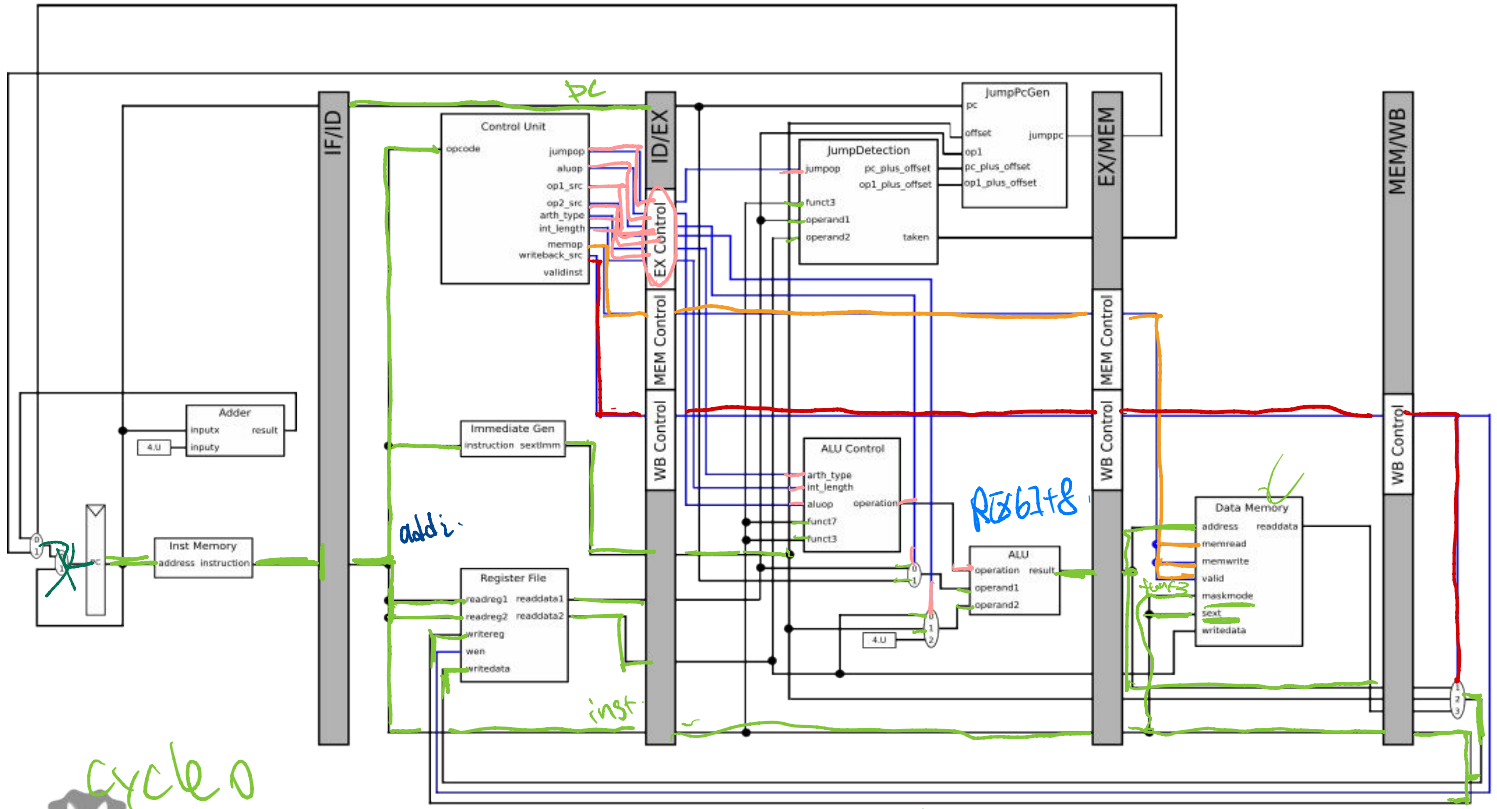
addi x5, x6, 8

nop

nop

nop

nop



cycle 0

cycle 1

cycle 2

cycle 3

cycle 4

Pipelined DINO CPU

Week 4

Question 1

The effective address is used to access memory

- execute
- fetch
- memory
- decode
- writeback

Question 2

The ALU generates a result value

- writeback
- execute
- memory
- fetch
- decode

Question 3

Bits from the instruction are used to choose which registers to read

- execute
- memory
- fetch
- decode
- writeback

Question 4

Retrieve 32 bits of data from memory which corresponds to the instruction

- writeback
- memory
- decode
- execute
- fetch

Question 5

The processor generates control signals for the instruction

- memory
- execute
- fetch
- decode
- writeback

Question 9

1 pts

[Select] is shared by all instructions.

[Select]
control path
data path

selects subsets of components to use for each instruction

data path

control path.

Question 10

1 pts

"A state element that contains a set of locations that can be read/written by supplying a location number and that is usually accessed multiple time for each instruction" describes which of the following data path elements?

- Immediate generator
- PC
- Muxes
- Instruction memory
- Register file
- ALU
- data memory
- control unit

Question 11 — 2 pts

There is a processor design that combines some steps. It has three stages: fetch & decode, execute, and memory & writeback. Use the following information to answer the question. Note: This may be different from other questions.

Fetch & Decode	Execute	Memory & Writeback
100ps	160ps	250ps

If this is a single-cycle processor design, what is the cycle time of this processor in ps?

100+160+250 = 510 ps.

Question 12 — 2 pts

There is a processor design that combines some steps. It has three stages: fetch & decode, execute, and memory & writeback. Use the following information to answer the question. Note: This may be different from other questions.

Fetch & Decode	Execute	Memory & Writeback
160ps	160ps	240ps

What is the CPI for this processor?

1.

Question 13 — 2 pts

There is a processor design that combines some steps. It has three stages: fetch & decode, execute, and memory & writeback. Use the following information to answer the question. Note: This may be different from other questions. 4.2

Fetch & Decode	Execute	Memory & Writeback
200ps	230ps	270ps

How long does it take to execute an application with 6 billion instructions on this single cycle processor (in seconds)?

exe time = #inst x CPI x cycle time.

$6 \times 10^9 \times 1 \times (200+230+270) \times 700 \times 10^{-12}$

= 4.2 s.

Question 14

1 pts

How long does it take to complete a single load of laundry (in minutes)?

Pre-wash Washing Drying Folding/hanging

50 min 60 min 50 min 60 min

50 + 60 + 50 + 60 = 220 min.

Question 15

1 pts

What is the limiting "stage" for this laundry system? (Can have multiple answers)?

Pre-wash Washing Drying Folding/hanging

40 min 60 min 40 min 50 min

- [ ] Pre-wash
- [ ] Drying
- [ ] Hanging/folding
- [x] Washing

Question 16

1 pts

What is the cycle time for the pipelined laundry (in minutes)? I.e., how frequently will a load be finished?

Pre-wash Washing Drying Folding/hanging

60 min 60 min 40 min 40 min

60 min.

Question 17

1 pts

What is the throughput for the pipelined laundry? I.e., how many loads can you complete **per hour**?

Pre-wash Washing Drying Folding/hanging

60 min 60 min 60 min 60 min

1

Question 18

1 pts

What is the speedup pipelining compared to not pipelining? Assume you only care about the steady state (i.e., no need to consider warmup/cooldown time).

Pre-wash	Washing	Drying	Folding/hanging
50 min	50 min	60 min	60 min

$\frac{(50+50+60+60)}{60} = \frac{220}{60}$

Question 19

How long does it take to execute a single instruction? (in ps)

Fetch	Decode	Execute	Memory	Writeback
600 ps	500 ps	400 ps	600 ps	400 ps

600 + 500 + 400 + 600 + 400.

Question 20

What is the limiting stage for this pipeline? (Can have multiple answers)?

Fetch	Decode	Execute	Memory	Writeback
500 ps	500 ps	200 ps	400 ps	400 ps

- [ ] Writeback
- [ ] Memory
- [x] Fetch
- [ ] Execute
- [x] Decode

Question 21

What is the cycle time for the pipelined processor?

Fetch	Decode	Execute	Memory	Writeback
600 ps	500 ps	200 ps	500 ps	400 ps

600 ps

Question 22

1

What is the throughput for the pipeline? I.e., how many instructions can you complete **per second**?

Fetch	Decode	Execute	Memory	Writeback
500 ps	300 ps	300 ps	500 ps	200 ps

2×10^9

$$\frac{1}{500\,ps}$$

Question 23

1 pts

What is the speedup pipelining compared to not pipelining? Assume you only care about the steady state (i.e., no need to consider warmup/cooldown time).

Fetch	Decode	Execute	Memory	Writeback
500 ps	400 ps	300 ps	500 ps	200 ps

$$\frac{(500+400+300+500+200)\,ps}{500\,ps}$$

Question 24

2 pts

For the following program mark the data dependencies. Put a check when the register listed after the : depends on one of previous (older) instructions `xori a5, t4, -1443`

```
sra a5, a2, a3
sll t0, a5, s3
slli t6, t0, 703
```

- [x] slli t6, t0, 703: t0
- [ ] xori a5, t4, -1443: a5
- [ ] sra a5, a2, a3: a2
- [ ] sll t0, a5, s3: s3
- [ ] sll t0, a5, s3: t0
- [x] sll t0, a5, s3: a5
- [ ] xori a5, t4, -1443: t4
- [ ] sra a5, a2, a3: a3
- [ ] slli t6, t0, 703: t6
- [ ] sra a5, a2, a3: a5

Question 25

2 pts

For the following program mark the data dependencies. Put a check when the register listed after the : depends on one of previous (older) instructions `addi a2, t6, 964`

```
add a2, a5, a3
sra t0, a2, t2
slli t3, t0, -20
```

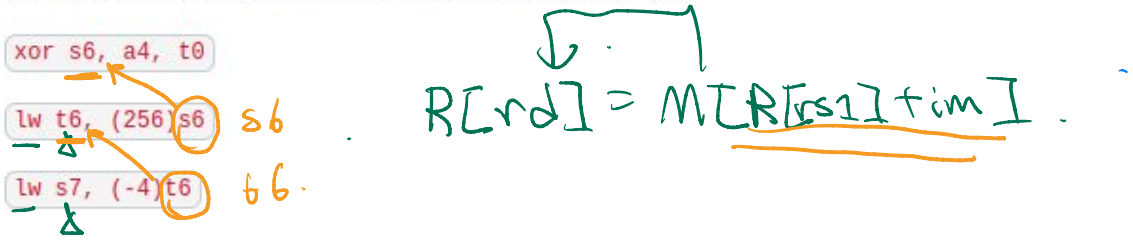
- [ ] add a2, a5, a3: a3
- [x] slli t3, t0, -20: t0
- [ ] slli t3, t0, -20: t3
- [ ] addi a2, t6, 964: t6
- [x] sra t0, a2, t2: a2
- [ ] add a2, a5, a3: a2
- [ ] addi a2, t6, 964: a2
- [ ] sra t0, a2, t2: t2
- [ ] sra t0, a2, t2: t0
- [ ] add a2, a5, a3: a5

Question 26

1 pts

For the following program mark the data dependencies. Put a check when the register listed after the : depends on a previous (older) instruction.

```
xor s6, a4, t0
lw t6, (256)s6
lw s7, (-4)t6
```



- [x] lw t6, (256)s6: s6
- [ ] lw s7, (-4)t6: s7
- [ ] xor s6, a4, t0: t0
- [ ] xor s6, a4, t0: s6
- [ ] lw t6, (256)s6: t6
- [x] lw s7, (-4)t6: t6
- [ ] xor s6, a4, t0: a4

Question 27

1 pts

For the following program mark the data dependencies. Put a check when the register listed after the : depends on a previous (older) instruction.

```
sra a6, t4, t5
sw a0, (-932)a6
sw a6, (496)a0
```

a6

a6

M[R[rs1]+imm] = R[rs2].

- [x] sw a0, (-932)a6: a6
- [ ] sra a6, t4, t5: a6
- [ ] sra a6, t4, t5: t5
- [x] sw a6, (496)a0: a6
- [ ] sw a6, (496)a0: a0
- [ ] sw a0, (-932)a6: a0
- [ ] sra a6, t4, t5: t4

Question 28

2 pts

Which of the following instructions will cause later instructions to stall assuming there's no branch predictor?

```
sub s11, s11, s6
jalr a4, s8, 1581
bne a7, a3, -1244
blt a2, s0, 1204
beq t1, t4, 545
jalr t2, s11, -1414
jalr s7, a6, 915
```

- [ ] `jalr a4, s8, 1581`
- [ ] `jalr t2, s11, -1414`
- [ ] `bne a7, a3, -1244`
- [ ] `blt a2, s0, 1204`
- [ ] `jalr s7, a6, 915`
- [ ] `beq t1, t4, 545`
- [ ] `sub s11, s11, s6`

Question 29

2 pts

Which of the following instructions will cause later instructions to stall assuming there's no branch predictor?

```
add s11, t0, a0
```

```
jalr t0, s1, 1405
```

```
jal t6, -1940
```

```
lw a4, -372(t4)
```

```
jalr s7, t1, 739
```

```
sll t6, s8, s8
```

```
xor t4, t3, s6
```

- [ ] `jalr t0, s1, 1405`
- [ ] `add s11, t0, a0`
- [ ] `jal t6, -1940`
- [ ] `jalr s7, t1, 739`
- [ ] `xor t4, t3, s6`
- [ ] `sll t6, s8, s8`
- [ ] `lw a4, -372(t4)`

Question 30

In which stage do you *know* you need to stall for a control hazard?

- ○ Writeback
- ✓ ○ Decode
- ○ Execute
- ○ Memory
- ○ Fetch

Question 31

When predicting a branch, you need to predict which two things:

- ✓ ☐ the target address
- ☐ if it is an exception
- ☐ forward or backward
- ☐ number of cycles to stall
- ✓ ☐ taken or not taken
- ☐ which stage it is in